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Research Article

A study of the silicon Bulk-Barrier Diodes designed in planar technology by means of simulation

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Abstract

In this paper, it is studied for the first time, the possibility of manufacturing a Bulk Barrier diode in planar technology using simulation. This study is based on simulation results obtained with a 2-D device simulator (S-PISCES). More precisely, the electrical and switching behavior of the proposed devices in planar technology were investigated. The results of this study show that the technological parameters (doping concentrations), as well as the geometrical sizes (middle region width) and the bias conditions (applied voltage), have significant effects on the electrical and switching behavior of the proposed devices. The appropriate choice of these parameters can reduce the switching time in the range of few picoseconds and also dramatically modify the current through the device. The simulation results of devices in planar technology have been compared with those designed in non planar technology. Finally, good agreement among theory and simulations results of the proposed devices observed.

Keywords: Device Simulation, electrical behaviour, Switching behaviour, Bulk-Barrier Diodes, planar technology.

1. Introduction

Bulk- Barrier Diodes (BBD's) [1, 2], or Camel Diodes (CD's) [3,4], are two - terminal three-layer structures similar to Bipolar Junction Transistor (BJT), where the current is controlled by a potential barrier located inside the semiconductor. However, contrary to the BJT's, the middle (base) region in BBD's is so thin that it is normally fully depleted from free carriers and there exists no neutral region. Similar structures appear in the literature with different names: "Bulk Unipolar Diodes" [5-7], "Triangular Barrier Diodes" [8], and "P-plane Diodes" [7]. All the above structures are, like Schottky diodes, in majority carrier devices and therefore can be used for high-speed applications. Contrary to the Schottky diodes, BBD's offer the possibility to control the barrier height by well controllable technological parameters, such as dopant concentration and middle layer width. This advantage over the classical Schottky diode makes them very attractive in many applications. There are several published works referring to the applications of such structures as photodiodes with high internal gain [4, 9], high speed optoelectronic switches [10,-16], temperature sensors [17], Bulk- Barrier Transistors [18], gates in FET's [19] and high speed devices [20]. All the above published works refer to devices that are designed in non planar technology.

In the present work we study for the first time the possibility of manufacturing a Bulk Barrier diode in planar technology using simulation. To be more specific, we investigate the electrical and switching behavior of devices in planar technology using advanced simulation packages (S-PISCES). The simulation results of devices in planar technology are given and compared to those in non planar technology. Additionally, the simulation results were used to verify the validity of the analytical model [2, 20] in the case of devices manufactured in planar technology.

2. Theoretical analysis

Fig.(1) shows the structure of the BBD in non planar technology and the distribution of space charge density, $\rho(x)$, electric field, $E(x)$ and electrostatic potential, $V(x)$, under equilibrium (———) as well as under forward (— · · —) and reverse bias conditions (— — —). Total depletion of the n layer, achieved by proper choice of the thickness and doping concentration of the middle layer, is a prerequisite for BBD operation [2]. It is also assumed that the three layers are uniformly doped with concentrations: N_C in the substrate layer (collector), N_B in the middle layer (base) and N_E in the surface layer (emitter). The solution of Poisson's equation in thermal equilibrium leads to a potential barrier height, Φ_{BL0}, given by:

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$$\Phi_{BL0} = V_B \cdot \left(1+\frac{N_B}{N_E}\right)\cdot\left(1+\frac{N_C}{N_B}\right) - \frac{N_C}{N_B}\cdot\left(1+\frac{N_B}{N_E}\right)\cdot V_D - -2\cdot V_B\cdot\left(1+\frac{N_B}{N_E}\right)\cdot\sqrt{\frac{N_C}{N_B+N_C}\cdot\left(1-\frac{V_D}{V_B}\right)} \quad (1)$$

With $V_B = \frac{q\cdot N_B\cdot d^2}{2\varepsilon}\cdot\left(1-\frac{\overline{n}_{B0}}{N_B}\right)$ (2)

where d is the middle layer thickness, q is the electron charge, $\overline{n}_{B0}$ is the electron mean density distribution in the middle layer, $\varepsilon = \varepsilon_0\varepsilon_r$ is the dielectric constant and V_D is the difference between the Fermi-level potentials in the p^+ and p layers and it is given by:

$$V_D = V_T \cdot \ln(N_E/N_C) \quad (3)$$

where $V_T = kT/q$. When the middle layer is fully depleted from free carriers Eq.(2) it takes the following form [2]:

$$V_B = \frac{q\cdot N_B\cdot d^2}{2\varepsilon} \quad (4)$$

Fig.(1d) shows qualitatively the variation of the potential barrier under bias conditions. For reverse bias (i.e. + on the emitter and – on the collector), the depletion layer width within the substrate expands and the potential barrier height on the right side of the middle layer Φ_{BR}, increases. At the same time the potential barrier on the left side Φ_{BL}, decreases, and so in this case the hole current over this barrier dominates. The opposite is valid for forward bias, where the hole current over the barrier Φ_{BR} dominates. Eq.(1) for Φ_{BL} under bias conditions takes the form:

$$\Phi_{BL} = V_B\cdot\left(1+\frac{N_B}{N_E}\right)\cdot\left(1+\frac{N_C}{N_B}\right) - \frac{N_C}{N_B}\cdot\left(1+\frac{N_B}{N_E}\right)\cdot(V_D \pm V) - -2\cdot V_B\cdot\left(1+\frac{N_B}{N_E}\right)\cdot\sqrt{\frac{N_C}{N_B+N_C}\cdot\left(1-\frac{V_D+V}{V_B}\right)} \quad (5)$$

where the ± signs are for the forward and the reverse bias conditions, respectively

Under forward bias conditions, the barrier height Φ_{BR} may be expressed in terms of the Φ_{BL} and the bias voltage by the equation:

$$\Phi_{BR} = \Phi_{BL} - (V_D + V) \quad (6)$$

provided that the applied voltage drops entirely in the collector junction.

Substituting Eq.(6) in Eq.(5) gives:

$$\Phi_{BR} = V_B\cdot\left(1+\frac{N_B}{N_E}\right)\cdot\left(1+\frac{N_C}{N_B}\right) - \left[1+\frac{N_C}{N_B}\cdot\left(1+\frac{N_B}{N_E}\right)\right]\cdot(V_D+V) - -2\cdot V_B\cdot\left(1+\frac{N_B}{N_E}\right)\cdot\sqrt{\frac{N_C}{N_B+N_C}\cdot\left(1-\frac{V_D+V}{V_B}\right)} \quad (7)$$

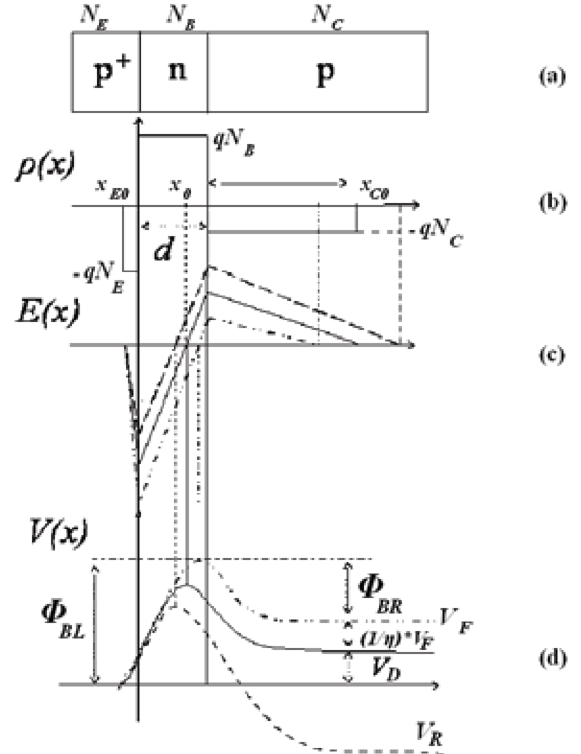


Figure 1. (a) Structure of the BBD, (b) space charge density distribution $\rho(x)$, (c) electric field distribution $E(x)$, and (d) electrostatic potential distribution $V(x)$, in thermal equilibrium (———), with a positive applied voltage (— · ·), and with a negative applied voltage (— — —).

Analytic Current – Voltage characteristics

The current in BBD's depend strongly on the mean free path of charge carriers. If the majority of charge carriers pass the potential barrier Φ without collision, the resulting current can be calculated based on the thermionic emission theory [3]. Otherwise, the drift-diffusion theory will apply [1]. In the intermediate case, the thermionic emission – drift-diffusion theory is valid [3]. All three theories define the current passing over a barrier as follows:

$$I = I_S \cdot \exp(-q\cdot\Phi/kT)\cdot[1-\exp(V/V_T)] \quad (8)$$

The current is an exponential function of the barrier height Φ, regardless of the mean free path of charge carriers. The difference between the various theories is expressed by the differences in saturation current I_S.

According to Eq.(8), carriers in a BBD that have to over-

come the lowest barrier contribute mostly to the current. In the forward bias the current through the diode is given by:

$$I_F = I_{SF} \cdot \exp\left(-\frac{q \cdot \Phi_{BR}}{kT}\right) \cdot \left[1 - \exp\left(-\frac{q \cdot V}{kT}\right)\right]$$

$$I_F = I_{SF} \cdot \exp\left(-\frac{q \cdot \Phi_{BR}}{kT}\right) \tag{9}$$

for $V > 3 \cdot \frac{kT}{q}$

where I_{SF} is the saturation current in forward bias given by:

$$I_{SF} = \frac{q \cdot N_C \cdot D_p \cdot A}{\sqrt{2\pi} \cdot L_D + \frac{D_n}{u_{th} / \sqrt{6\pi}}} \tag{9.1}$$

where A is the cross-section area, D_p and D_n are the diffusion coefficients for holes and electrons, respectively, L_D is the Debye length, and u_{th} is the thermal velocity.

Following the same procedure, as for Eq.(9), the reverse bias current can be expressed by:

$$I_R = I_{SR} \cdot \exp\left(-\frac{q \cdot \Phi_{BL}}{kT}\right) \cdot \left[1 - \exp\left(\frac{q \cdot V}{kT}\right)\right] \tag{10}$$

Where I_{SR} is the saturation current in reverse bias given by:

$$I_{SR} = \frac{q \cdot N_E \cdot D_p \cdot A}{\sqrt{2\pi} \cdot L_D + \frac{D_n}{u_{th} / \sqrt{6\pi}}} \tag{10.1}$$

From Eq.(9.1) and (10.1) it is obvious that

$$\frac{I_{SF}}{I_{SR}} \cong \frac{N_C}{N_E}$$

Switching behavior analytical model

For switching applications, the transition from a conducting to a non-conducting state (e.g. from forward to zero bias) must be nearly abrupt and the transient time must be short. In the case of a Bulk Barrier Diode (BBD) when the bias voltage is switched from a forward voltage V_F to zero voltage, the current through the diode changes abruptly from I_F to a reverse current I_R which afterwards decays exponentially to I_S within a certain time. The switching time is defined as the time in which the device current reaches 10% of its initial value I_R. Several mechanisms can extend this switching time. According to [20] the total switching time for BBD's is given by:

$$\tau_{SW} = \tau_{STOR} + \tau_{TRAP} + \tau_{TRAN} + \tau_{RC} \tag{11}$$

Where:

τ_{STOR} is the storage time of minority carriers (electrons) on the edges of the depletion region, τ_{TRAP} is the trapping time of free electrons in the potential well, τ_{TRAN} is the transit time of free carriers travelling through the depletion region and τ_{RC} is the depletion layer discharging time. This is the time required to discharge the depletion capacitance C_D, through a finite resistance R ($\tau = R * C_D$).

According to [20] the switching time of BBDs is mainly determined by the depletion layer discharging time. This is associated with the finite time that takes to modulate the space charge in the depletion region. This has to be done by injecting an input current that discharges the depletion capacitance C_D, through a finite resistance R. Therefore the total switching time for BBDs is given by:

$$\tau_{SW} = 2.3 \cdot R \cdot C_D \tag{12}$$

Eqs. (9) and (10) show that the current through the BBD increases exponentially with the applied voltage in both bias conditions. This is valid only for the case in which the injected carrier charge in the depletion region remains low compared to the space charge (low injection). In the case in which the injected carrier charge becomes significant (high injection), the dynamic resistance (junction resistance) R_D assumes very small values compared to those of the series resistance R and most of the applied voltage drops across R_S. In this way, the exponential dependence of current from applied bias voltage changes initially to saturation and then to a linear law. High injection dominates when the current determining barrier becomes very low. This can occur either for large values of the applied voltage or for small values of the middle region thickness (d) or dopant concentration (N_B) (eqs(1-6)). In the latter case, the potential barrier formed is too low to maintain a depletion region empty of carriers, even for small values of the applied voltage.

According to the equivalent circuit of a majority carrier device in the case of the depletion capacitance discharge [21], where the applied voltage is equal to zero, the resistance R is the parallel combination of the series resistance R_S and of the dynamic (differential) resistance R_D. It is given by:

$$R = \frac{R_S \cdot R_D}{R_S + R_D} \tag{13}$$

$$R_S = \rho \cdot \frac{l}{S} = \frac{1}{q \cdot \mu_p \cdot p} \cdot \frac{l}{S} = \frac{1}{q \cdot \mu_p \cdot N_C} \cdot \frac{l}{S} \tag{14}$$

$$R_D = (\partial I / \partial V)^{-1} = \frac{\eta \cdot kT/q}{I} \tag{15}$$

Where l is the substrate thickness S is the device cross-sectional area, ρ is the resistivity, μ_p is the hole mobility of the substrate and η is the diode ideality factor [1, 2].

The depletion region capacitance C_D is the series combination of the emitter – base capacitance C_{EB} and the base- collector capacitance C_{BC} and can be expressed by:

$$C_D = \frac{C_{EB} \cdot C_{BC}}{C_{EB} + C_{BC}} \tag{16}$$

with

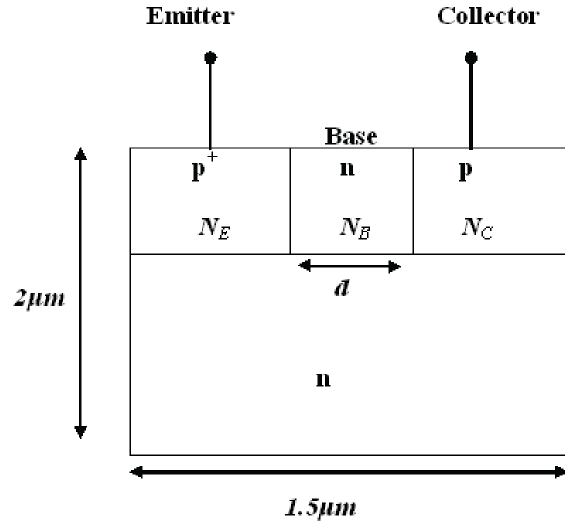
$$\left.\begin{aligned} C_{EB} &\approx \left(\frac{\varepsilon_r \cdot \varepsilon_0 \cdot q \cdot N_B \cdot S^2}{2 \cdot \Phi_{BL}} \right)^{\frac{1}{2}}, \text{for } N_B/N_E \ll 1, \text{ and} \\ C_{BC} &\approx \left(\frac{\varepsilon_r \cdot \varepsilon_0 \cdot q \cdot N_C \cdot S^2}{2 \cdot \Phi_{BR}} \right)^{\frac{1}{2}}, \text{for } N_C/N_B \ll 1 \end{aligned}\right\} \tag{17}$$

It is obvious from eqs. (13) and (16) that the smallest resistance and the smallest capacitance determine the switching time τ_{SW} and is strongly affected by the substrate dopand concentration N_C [20]. Thus, by the proper choice of N_C, the switching time can be reduced in the range of picoseconds.

3. Simulation results and discussion

Fig.(2a) shows the proposed structure of the BBD in planar technology. The three regions are uniformly doped with the following concentrations: N_C in the p type region (collector), N_B in the n type region (base) and N_E in the p+ type region (emitter). These thee regions are deposited on an n- type Si substrate. Total depletion of the n type region, which is a prerequisite for BBD operation, is achieved by the proper choice of thickness and doping concentration of the n type region. In order to investigate the electrical and the switching behavior of the proposed structure, advanced simulation programs such as S-PISCES (SILVACO) which work under ATLAS framework, were used. Fig. (2b) shows the resulting simulated structure of the BBD in planar technology.

ATLAS is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations derived from Maxwell's laws onto this grid you can simulate the transport of carriers through a structure. The S-PISCES is a 2-D device simulator that simulates the electrical characteristics of silicon semiconductor devices in steady-state, transient and AC conditions. The device structures in S-PISCES may be specified by the user. For the simulation, the drift-diffusion model was used, because the geometrical characteristics of the structures were much larger than the mean free path of carriers. In addition, for more accurate predictions of device performance, several physical models, such as concentration and field dependent mobility, Shockley-Read-Hall and Auger carrier recombination and band gap narrowing were employed.



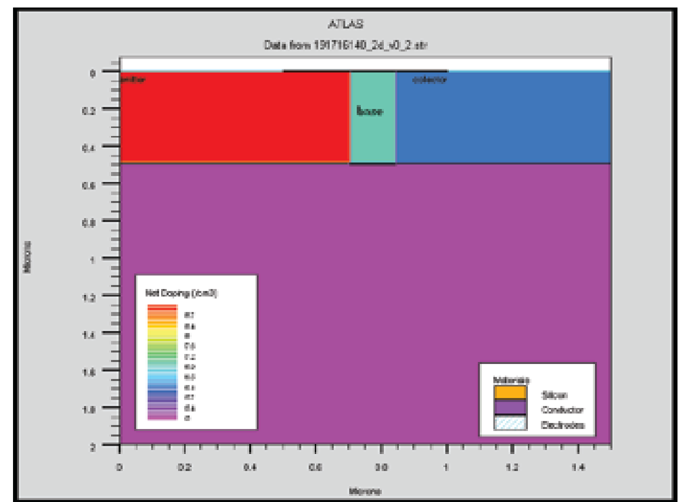


Figure 2. Schematic representation of a p+-n-p structure in planar technology (a). S-PISCES structure of a p+-n-p structure in planar technology (b).

Fig. (3) shows the simulation results of the net doping, free hole and free electron concentrations profiles (3a), the electric field, $E(x)$ (3b) profile and electrostatic potential, $V(x)$ (3c) profile, along the x direction of the proposed device under zero bias conditions. These results are in good agreement with the theoretical profiles shown in Fig.(1). The free electrons concentration in the n region of the proposed device, as Fig.(3a) shows, is lower than the donor concentration (~ 10^{14} cm^{-3}) and therefore, this region is almost depleted even for very small values of applied bias voltage. In this case the proposed device with the corresponding technological parameters (N_E=10^{19}cm^{-3}, N_B =10^{17}cm^{-3}, N_C =10^{16}cm^{-3}, d=120nm) is working as a BBD structure [2].

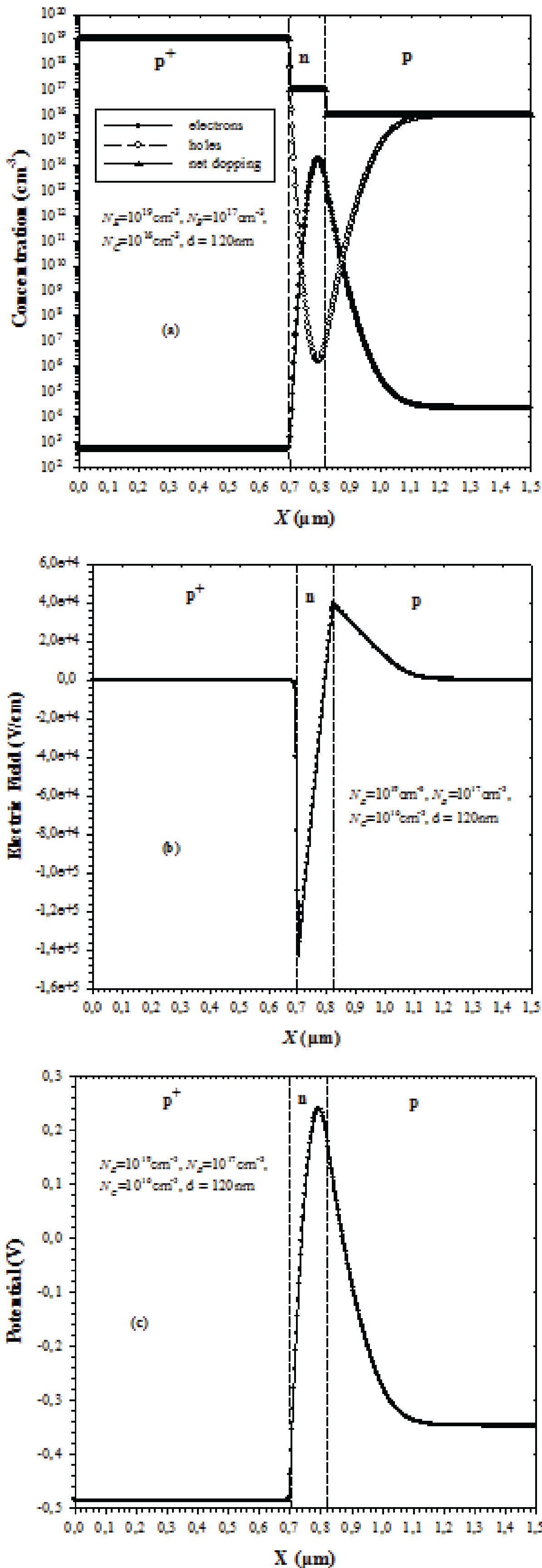


Figure 3. S- PISCES data of net doping, free electron and hole concentrations ($n(x)$, $p(x)$) (a), electric field $E(x)$ (b) profile and electrostatic potential $V(x)$(c) along the x(μm) direction along in the proposed BBD device under zero bias conditions.

Figs. 4 (a and b) show the simulated I-V characteristics of the proposed BBD device in planar technology with N_E=10^{19}cm^{-3}, N_B =10^{17}cm^{-3}, N_C =10^{16}cm^{-3} and different middle region thicknesses d under forward and reverse bias conditions. The values of d were chosen to demonstrate the various operations of the devices. Thus for d=80nm, the I-V characteristics saturate even for low values of the applied voltage, because the structure in this case operates like p+- p junction [2]. I-V curves for d=150nm and 200nm indicate that the BBD operation begins at about 0.3V and 0.5V respectively. For voltages less than these values the current slightly increases with the voltage, because the free electron concentration in the middle region is very close to the donor concentration. Thus, a neutral zone appears in the middle region and the current is limited by a recombination mechanism. As the voltage increases the free

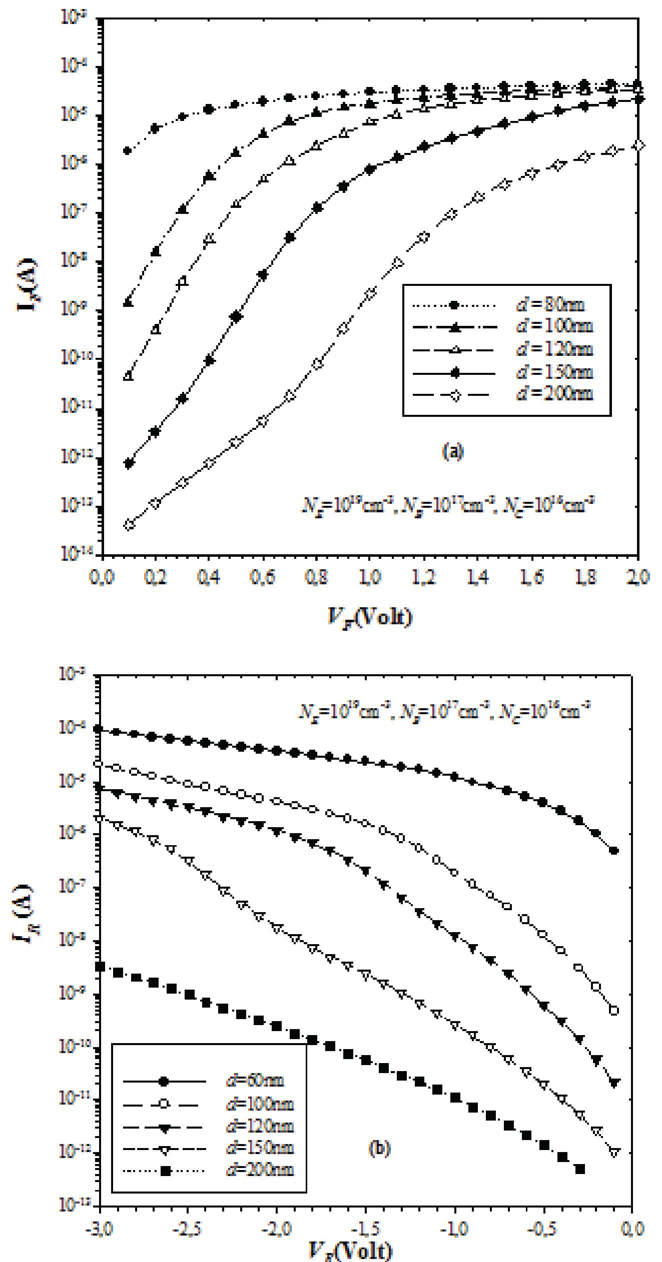


Figure 4. S-PISCES data for Current – Voltage characteristics of the proposed BBD structure in planar technology with different d under forward (a) and reverse (b) bias conditions.

electron density decreases exponentially, so that the neutral zone disappears and the current increases abruptly. For d=100nm and 120nm the structures operate as BBD's for any forward bias voltage applied, because the electron concentration in the middle layer is lower than the donor concentration and, therefore, this region is almost depleted even for very small values of applied bias voltage.

The reverse I-V characteristics are shown in Fig.4(b). For d=100nm and 120nm, the current rises with applied reverse bias voltage. For d=150nm and 200nm, the current rises slowly with the applied reverse bias voltage, because of the high free electron concentration in the middle layer and the formation of a neutral zone in this region. These simulated I-V characteristics of the proposed BBD structure in planar technology are in good agreement with the theoretical model.

In order to compare the two different design technologies, planar and non-planar, Figs. 5 (a, b) present the simulated I-V characteristics of BBD structures designed in non-planar technology, Fig. 1(a). It is obvious that in Figs.4 (a, b) and Figs.5 (a, b) the same operation, for the different values of d is observed.

Figs. 6 (a, b) show the simulated I-V characteristics of the proposed BBD device in planar technology with N_E=10^{19}cm^{-3}, N_B =10^{17}cm^{-3}, d=100nm and different collector concentration N_C (p type region), under forward and reverse bias conditions. According to theoretical model, (Eqs. (5) and (7)) the barrier height in the forward Φ_{BR} and reverse Φ_{BL} bias conditions, are significantly influenced by the values of the N_B and N_C concentrations. Thus for large values of N_C, the current increases in both bias conditions and goes into saturation even for low values of the applied voltage, because the corresponding barrier height Φ_{BR} or Φ_{BL} decreases [2]. For lower values of N_C the current takes lower values

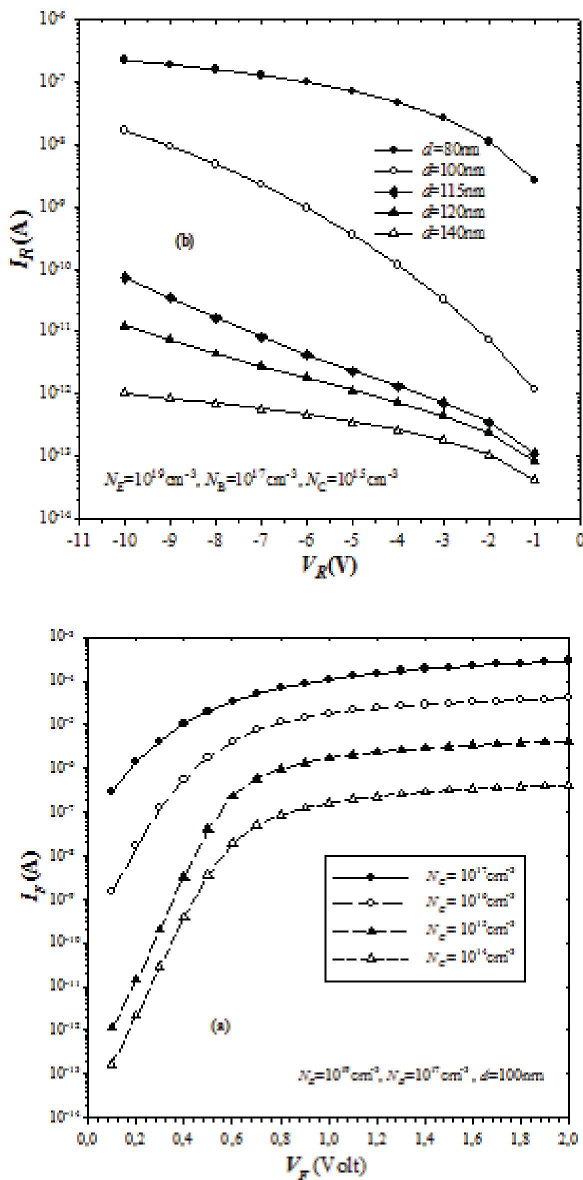


Figure 5. S-PISCES data for Current – Voltage characteristics of a BBD structure in no planar technology with different d under forward (a) and reverse (b) bias conditions.

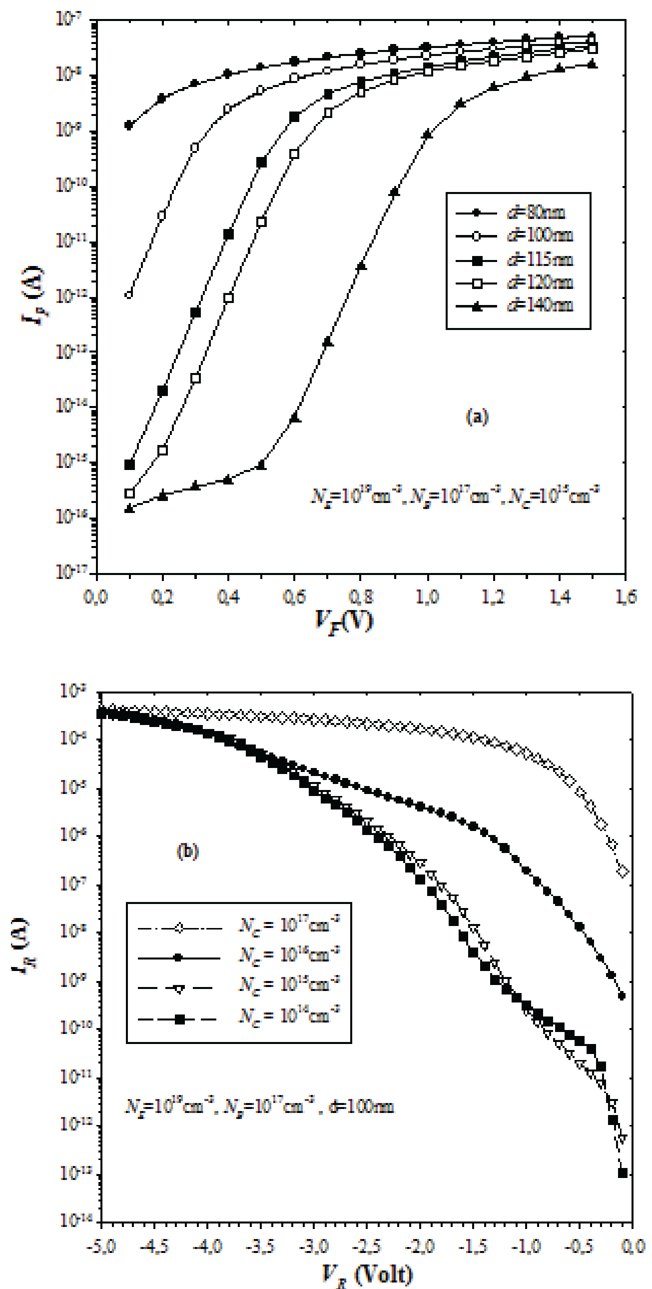


Figure 6. S-PISCES data for Current – Voltage characteristics of the proposed BBD structure in planar technology with different collector concentration N_C (p type region), under forward (a) and reverse (b) bias conditions.

and the corresponding devices are working as BBD structures.

The proposed device in planar technology operates like BBD devices designed in non-planar technology. As the proposed structures designed in planar technology have the advantages of the BBD operation [1, 2], makes them attractive in applications such as gates in FETs or FinFETs, where current control is needed [22, 23].

The BBD structures as majority carrier devices, similar to Schottky diodes (i.e. not exhibiting minority carrier charge storage in the quasi-neutral regions) can be used for high-speed applications, thus the switching behaviour of these structures was also investigated. More specifically, the influence of various technological parameters on the switching behaviour of the proposed structure were investigated by means of simulation.

The simulation results of the collector current response when the applied bias switched between 1V to 0 V, is presented in Fig.7, for a structure with N_E=1019cm-3, N_B=1017cm-3 and d=120nm. It is obvious from this figure that when the bias voltage is switched from a forward voltage equal to 1V to zero voltage, the current through the structure changes abruptly from I_F to a reverse current I_R which afterwards decays exponentially to I_S within a certain time. The switching time τ_{SW} for this structure is equal to 9.4 psec.

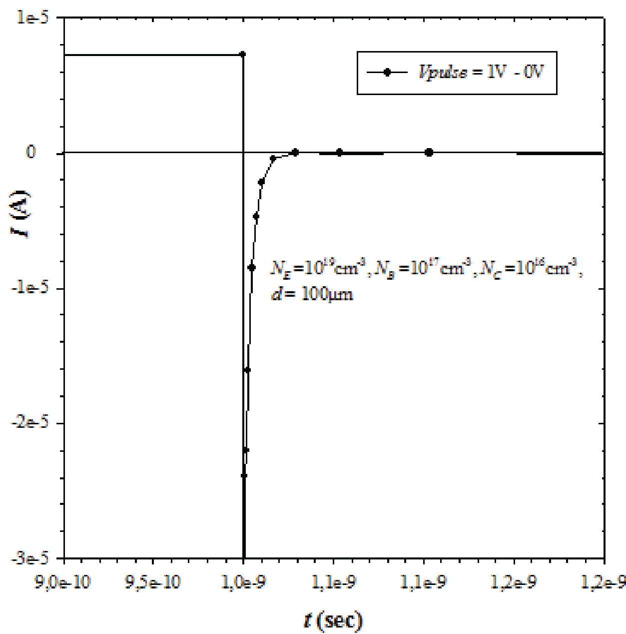


Figure 7. Simulation results of the collector current response when the applied bias switched from 1V to 0 V, for a structure with N_E = 10^{19}cm^{-3}, N_B=10^{17}cm^{-3}, N_C=10^{16}cm^{-3} and d=120nm.

In Fig. 8, simulation results for the switching time τ_{SW} as a function of the middle region thickness d, is presented. In this case, the quantities N_E, N_B and N_C were held constant. The applied voltage was switched between forward and zero bias. As it can be seen from Fig. 8, τ_{SW} exhibits different dependences with respect to variable d similar to these observed for structures designed in no planar technology [20]. The switching time τ_{SW} exhibits a maximum. On the left and right of this maximum, τ_{SW} decreases and, finally on the right it saturates. The saturation on the right side is due to the saturation of the potential barrier Φ_{BL0}. In this case, a neutral zone is created in the base and the structure operates like a BJT [2]. As the middle region width decreases, Φ_{BL0} becomes gradually low and according to Eqs. (1) and (17), both capacitances C_{BC} and C_{EB} increase. Because the barrier is still relatively high, the dynamic resistance R_D remains large and it does not affect significantly the total resistance of the device ("low injection" condition). Thus, τ_{SW} increases to, following the dependence of C_{BC} on d. As d continues to decrease, the zero potential barriers become gradually lower and the corresponding current becomes larger. Gradually the device falls into the "high injection" condition, where R_D becomes very small and it dominates in comparison with R_S. In this region, the switching time follows the dependence of R_D which, according to the eqs. (1), (15) and (9), decreases by decreasing d. It is obvious that the maximum value of the switching time τ_{SW} is due to the "high" and "low" injection conditions.

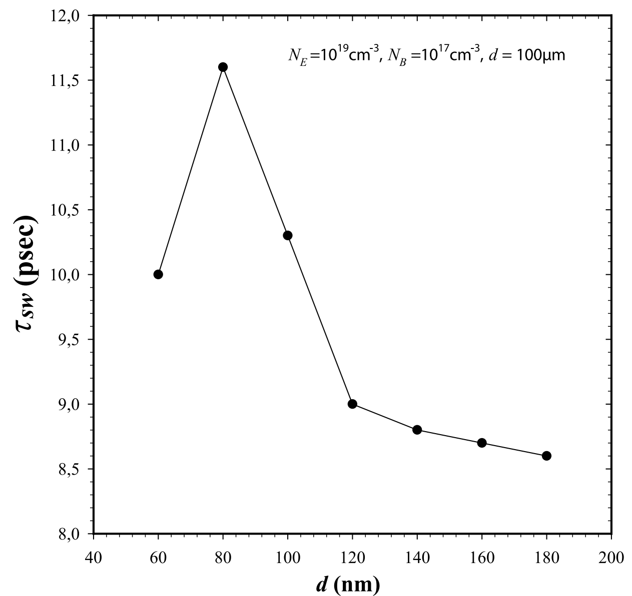


Figure 8. Influence of the middle layer thickness, d, on the total switching time τ_{SW} (data obtained from S- PISCES).

Another significant technological parameter which affects the switching time of proposed BBD structures designed in planar technology, is the collector dopand concentration N_C (p type region). Fig. 9 shows the simulation results of τ_{SW} versus N_C, for different structures with the same middle region thickness d (d=100nm). The applied voltage for all structures was switched between 1V and zero bias. It is obvious from Fig. 9 that τ_{SW} decreases by increasing the collector dopant concentration N_C. Considering that the proposed structure with d=120nm operates in "low injection" conditions, the dominant resistance and capacitance in the transient process will be R_S and C_{BC}, respectively. Thus, according to Eqs. (14) and (17), the resulting time τ_{SW} should be inversely proportional to the square root of the substrate dopant concentration. Indeed Fig.9 shows that for large values of N_C (i.e. for NC > 10^{15}cm^{-3}), τ_{SW} decreases linearly with a constant slope of -0.5 (on a log-log scale graph). For lower values of N_C (i.e. for N_C<10^{15}cm^3), the switching time τ_{SW} slightly changes, because as N_C decreases, the depletion regions of the corresponding devices increase. Further increase of the depletion region is limited

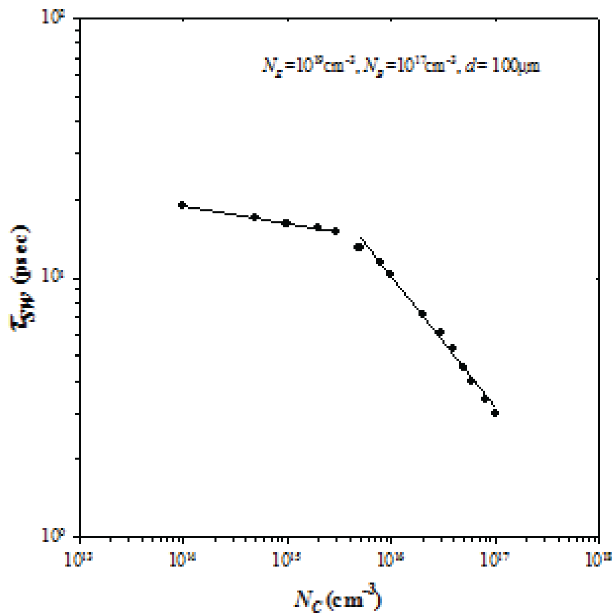


Figure 9. Influence of the collector dopant concentration, N_C, on the total switching time, τ_{SW}, for different structures with d=100nm (data obtained from S- PISCES).

by the geometry of the device. Finally, it is evident from Fig.9 that by the proper choice of the technological parameter N_C, we can reduce switching time of the proposed structures in the picoseconds range ($\tau_{SW}\approx$1 or 2 ps).

4. Conclusions

In this paper, we have proposed a p+-n-p structure designed in planar technology using simulation. We investigate the electrical and switching behavior of the proposed structures. The simulation results show that he proposed structure operates like a typical a Bulk Barrier diode.

More specifically, taking into consideration the electrical behavior, the main conclusion are:

- The barrier height is mainly a function of the N_B, N_C and of d; the limits of BBD operation can be controlled by the values of d and N_B, for given values of N_E and N_C.
- The collector dopant concentration N_C, strongly affects the current through the structure in both bias conditions.
- Barrier height engineering can easily be achieved by the appropriate choice of technological parameters.

Concerning the switching behavior, the main conclusion are:

- The proposed structures, as majority carrier devices, exhibit no minority carrier storage effect and, therefore, can operate with inherently fast response.
- The switching time of the proposed structure is mainly determined by the depletion layer discharging time (τ ~ RC).
- The switching time is a function of the technological parameters N_B, N_C and d and, thus, by the appropriate choice of these parameters, the switching time can reach the range of few picoseconds ($\tau_{SW}\approx$1 or 2 ps).

As the proposed structures have the advantages of the BBD operation [2] and can be designed in planar technology, makes them attractive in many applications such as gates in FETs or FinFETs where current control is needed [22, 23] or as high speed devices in IC technology.

Acknowledgments

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