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Synchronization and Calibration FPGA design for the XG-PON Optical Network Unit & Terminals (ONU/ONT)

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Abstract

The XG-PON standard for Passive Optical Networks (PONs) imposes requirements for high performance network equipment architectures. Especially, the 10G receiver of the ONU/ONT becomes quite demanding. The current paper proposes an efficient architecture for the synchronization and the calibration processing blocks of the ONU/ONT receiver. The proposed architecture process in parallel words of 64 bits and it achieves the calibration of the receiver in 2ms. The design uses fragments of 16 bits for comparison with the synchronization pattern (Psync) to improve the combination of hardware resource utilization and time response. This work verifies the performance of the design on a Xilinx Virtex 7.

Keywords: XG-PON, ONU/ONT, Synchronization, Calibration, FPGA.

1. Introduction

The evolution of the PON technologies and the design of Fiber-To-The-Curb (FTTC) network architectures target the ability of universal communication with increased capacity for a large number of connected users, offering at the same time enhanced security and services. To this respect, the latest XG-PON standard [1]has defined the network downstream/upstream traffic to reach 10Gbps and 2.5Gbps respectively. Hence, the corresponding XG-PON systems, which realize the functions of the Optical Line Terminal (OLT), the Network Unit (ONU) and the Terminal (ONT), have to perform high speed calculations on data with word length either32 or 64 bits.

In the last decade a variety of solutions for the ONT and ONU designs have been introduced by authors in the academia[12], [13], [8] and the industry[14], [15], [4], [5], [6], [9] based on different approaches. Apart the innovative features of each approach, the complexity of certain blocks remains high. Among the most complicated blocks in all design approaches remains the receiver (Rx) because it has to handle 10Gbps downstream traffic. Moreover, the industry imposes the requirement for low cost implementation. The current paper presents an approach for designing two of the most demanding components, which are a part of the physical adaptation layer processing in the receiver: the calibration and the synchronization processing block.

The receiver of the XG-PON physical a

daptation layer [1]has input frames of constant size and duration 125us and at the rate of 9.95328 Gbps it translates to 38880 words of 32 bits (or 19440 words of 64 bits).Hence, the synchronization and the calibration processing blocks of the receiver, are required to perform either in a very high speed or process in parallel a large number of bits (32 or 64 bits).The first six 32-bit words of the input frames are unscrambled in order to synchronize the receiver[1].The proposed architecture includes a Serializer/Deserializer (SERDES)to shape the input bit-stream into a 2-word (64 bit parallel) format and it communicates these 2-word structures to the other Rx blocks through a 64-bit parallel bus with operating frequency 155.52 MHz. The present paper proposes an efficient architecture for realizing these processing blocks which process 64 bits in parallel. The design targets an FPGA implementation and it has been realized on a Xilinx VC707 evaluation board. Fig. 1 depicts the overall architecture of the frame synchronization of the Rx as well as the required blocks that complete the design:

1. An optical module (SFP+).
2. The FPGA transceiver (Xilinx GTX) involving an integrated serializer/deserializer.
3. The calibrator block, which handles the alignment of the words that are the output of the deserializer.
4. The synchronizer block, which expects the synchronization pattern (Psync) at the start of each frame.
5. The decoding and the processing blocks.

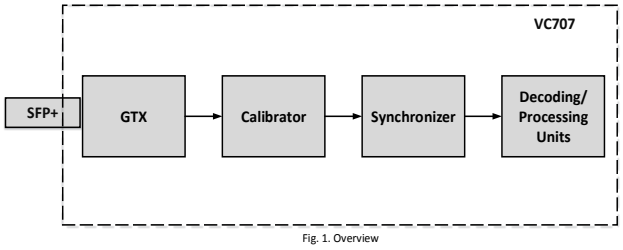

Fig. 1. Overview

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This work focuses on the design of the calibrator and the synchronizer blocks and their interaction with the other blocks of the receiver. The proposed Calibrator and Synchronizer process two words of 64 bits in parallel to keep the operating frequency at 155.52 MHz. The design is scalable and it is implemented and validated on the Xilinx Virtex-7 FPGA (VC707) occupying 314 slices and consuming 5.2 mW. The design of the synchronization block exploits the periodic nature of the XGTC frames. The repetition of the synchronization pattern in constant intervals allows the proposed synchronization blocks to operate only when the synchronization pattern is received. The stall of the synchronization blocks operation keeps the power consumption at relatively low levels.

This paper is organized as follows: Section 2 provides a description of the functionality of the two blocks. Section 3 describes the architecture details and the functionality of the calibrator and synchronizer blocks. Section 4 presents details of the FPGA implementation and finally, section 5 concludes the paper.

2. Overview of the Calibrator & Synchronizer Blocks and their Functionality in the ONU/ONT receiver

The calibration and the synchronization blocks belong to the receiver of the XG-PON ONU/ONT and they are placed between the SERDES and the decoding modules. These two blocks operate continuously during the synchronization phase; and after the completion of synchronization they operate only during the reception of the Physical Synchronization Block downstream (PSBd) of each frame. Fig. 1 depicts these blocks within the ONU/ONT receiver. The ONU's receiver gets as input from the ODN a bit-stream with the rate of 9.95328 Gbps. The SERDES transforms the serial bit-stream into contiguous words of 64-bits. The role of the calibrator is to formulate the 64-bit words as these were sent by the OLT transmitter (calibration):that is to locate the first bit of each 64-bit word. It accomplishes this task by changing the choice of the first bit of the 64-bit word. When the calibration process is completed, the synchronizer takes as input the 64-bit words that are the output of the calibrator. The synchronizer's role is to identify the Psync (synchronization pattern), create control signals for the rest of the ONU and check if the synchronization is maintained during the ONU's operation. The following sections present the architectural details of these two blocks.

3.Calibrator and synchronizer blocks

3.1. Calibrator

The deserialization process performed by the transceiver's SERDES consists of choosing one bit as the starting bit of a 64-bit word and to continue reading the input bit-stream as contiguous 64-bit words. The choice of the first bit is called word alignment. The role of the calibrator is to check if the 64-bit words are the same as they were sent by the OLT .It accomplishes this task by comparing the words to the Psync pattern. If the SERDES output does not match the OLT's word formulation then the calibrator will instruct the SERDES to choose another bit for a word start or in other words to shift the word start by one bit. Our approach, described below, exploits the periodic nature of the downstream XGTC frames.

The calibrator stores the synchronization pattern (0xc5e51840fd59bb49) in a register. It uses this register to check if under the given word alignment it is possible to detect the Psync pattern in any of the input words. It repeats the above checking for a period of time, which equals the size of the XGTC frame. If the calibrator does not detect the Psync pattern within this period, it will activate the *slip* signal, which will cause the shift of the deserializer's parallel output (choose another bit for word start).When the calibrator detects the sync pattern it keeps the *slip* signal disabled until the next system reset.

To speed-up this process and at the same time keep the power consumption low, we use a circuit with three cascaded registers R_1, R_2, R_3.Also, each of these three registers R_i ($1 \leq i \leq 3$) is divided into four fragments of 16 bits. We denote each fragment by R_{ij}, $0 \leq j \leq 3$.The architecture includes a circuit that can realize the mapping of four contiguous fragments of the concatenated R_2, R_1 onto R_3, that is any of: R_{20}, R_{21}, R_{22}, R_{23} or R_{21}, R_{22}, R_{23}, R_{10} or R_{22}, R_{23}, R_{10}, R_{11}or R_{23}, R_{10}, R_{11}, R_{12} can be mapped onto R_{30}, R_{31}, R_{32}, R_{33}.

The above circuit instructs the registers R_2 and $R_1$to contain two contiguous 64-bit words of the input. The calibrator checks if the 16 first bits of the Psync pattern match with any of the bit strings stored in the fragments of R_{20} or R_{21} or R_{22} or R_{23}. If the result is positive then it has a partial match of the Psync. To complete the matching process, it formulates the 64-bit word located in the concatenated R_2, R_1 starting with the fragment of R_2 where the partial match was found. If the match of the 64-bit word with the Psync pattern is successful, then we consider that the mapping circuit will lock and it will keep mapping the particular concatenation format onto $R_3$for the remaining of the ONU operation (until the next reset or synchronization loss). Hence, R_3will provide to the other circuits of the ONU receiver the correct 64-bit input words.

The process described above assures that the calibration will be achieved at most in 2ms (16 XGTC frames received). This technique is advantageous compared to the straightforward matching of the 64 bits register R_1 to the 64-bit input words. The latter is area efficient because it needs only the 64-bit comparator; the disadvantage of this approach is that in the worst case the calibration would be achieved in 8ms (64 XGTC frames received).

Fig. 2 depicts the architecture of the calibrator block. The counter of Fig. 2 starts its operation when the first 64-bit word is received and it will be reset each time its value equals the size of one XGTC frame. In this case it has either detected the Psync or failed to detect it. In the case of failure the control unit will assert the *slip* signal. Upon the first successful match the control unit will instruct the concatenation circuit to lock: the circuit will keep the mapping of the concatenated fragments of R_2, R_1 onto R_3(that is to keep the same input formulation into a 64-bit word). Also, it will keep the *slip* signal inactive until the reset of the system.

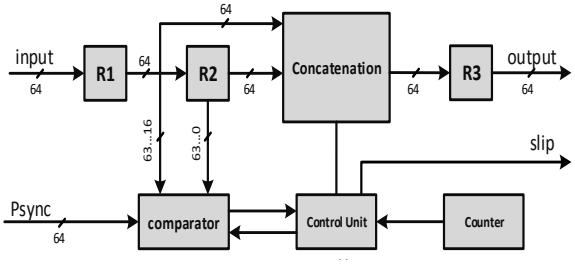

Fig. 2. Calibrator

3.1. Synchronizer

The synchronizer begins its operation when the calibration process has been completed successfully. The input of the synchronizer is the 64-bit words that are the output of the calibrator. When the synchronization pattern (Psync) is detected, a signal (*valid* signal) indicating that the ONU is receiving valid XGTC frames will be asserted and it will remain active until the next synchronization loss. Every 19440 64-bit words (the size of one XGTC frame)the synchronizer checks if its input matches the synchronization pattern. If the match is not successful it will be assumed that the synchronization is lost. When the synchronization is lost the valid signal will be inactive and the ONU will discard the received XGTC frames. If the synchronization is lost the above process will be repeated. The *start of frame* signal is asserted every time the synchronization pattern is detected and it is used as the indication of the beginning of a new frame. The *start of frame* signal is utilized by the other blocks of the ONU.

Fig. 3 depicts the architecture of the synchronizer. The Psync pattern is stored in a register and the comparator is checking if the register contents match the input word. To improve the power consumption after the first successful match the comparator is operating only when the counter equals the size of the XGTC frame. The decision unit is responsible for activating/deactivating the control signals(valid, start of frame) depending on its inputs from the counter and the comparator. The start of frame signal is asserted when the counter equals the size of the XGTC frame and the comparator has matched successfully the input word with the Psync pattern. Also the decision unit activates and deactivates the valid signal depending on its current status and the result of the Psync comparison. This signal is also used to inform the other modules of the ONU that the ONU is still in operating mode.

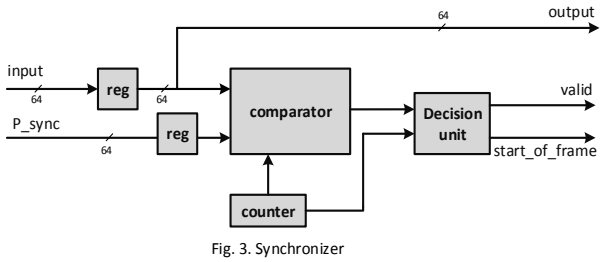

Fig. 3. Synchronizer

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4.FPGA Implementation

The XG-PON synchronization & calibration blocks have been implemented on the Xilinx VC707 evaluation board. Both the synchronizer and the calibrator were designed using synthesizable VHDL code. TABLE 1 displays the logic utilization of distinct modules on the Virtex 7 FPGA. For the ONU receiver we have used a Xilinx GTX connected to a SFP+ optical transceiver to achieve 9.95328 Gbps. For testing purposes we have also developed an OLT transmitter which includes only the necessary functionality for generating testing sequences.

Table 1. FPGA Utilization Virtex7 VC707

Implementation Results	Calibrator	Resources Utilization (Calibrator)	Synchronizer	Resources utilization (Synchronizer)
Slice LUTs	340	1%	199	1%
Slices	182	1%	98	1%
Slice Registers	251	1%	88	1%
Frequency (MHz)	268.456	-	194.060	-
Power Consumption (mW)	1.9	-	3.2	-

5.Conclusions

The current paper has presented an architecture for the calibrator and synchronization blocks of the XGPON ONU/ONT receivers; and it proposed a technique for the synchronization pattern matching based on fragment matching. The proposed technique improves the combination of the time required for calibration and synchronization and the required FPGA resources.

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