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Coordinate Logic Order Statistics filters and FPGA Implementation for Real-Time Image Processing

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Abstract

Coordinate Logic Order Statistics (CLOS) constitutes a new revolutionary and radical approach for real time video/image/signal processing. CLOS filtering introduces a minimalistic approach for filter design followed with the most possible efficiency in terms of performance, output quality, H/W complexity and energy consumption. More specific CLOS filters consider the signal values as fixed, unsigned and unweighted binary sequences without including carry bits and pointers. CLOS functioning applies a bit level process rather than a decimal level process and may be considered as a bottom up procedure where the whole filter design is based on logic functions instead of arithmetic. This feature is very important since it makes CLOS filters ready for "feeding" H/W. An example of an impulse denoising filter using CLOS is presented.

Keywords: Real Time Image and Signal Processing, Order Statistics, Signal Depended Median.

1. Introduction

The need for embedded real time image/video processing has brought the hardware design at its limits, while the innovation of new H/W, materials and VLSI approaches is very expensive. The problems that modern microelectronics face are not only miniaturization but also energy consumption. Moreover, although our computational machines are powerful we are not able to satisfactory implement tasks that biological organisms do (for example image recognition/ interpretation).

These problems arise in many modern applications, for example defense applications require very high performance computations (process a frame-by-frame 720p video input stream at 60 frames per second!) and have limited space for hardware, dictating a small system size. This requires a solution with good heat dissipation and the ability to consistently operate at low power. Similar problems and challenges arise every day in many fields such as industrial automation, automated surveillance, image recognition, automated video indexing, biometrics, neuroprosthetics, medical, web video streaming and mobile communications. In order to solve these challenges, more sophisticated image processing algorithms must be designed in order to reduce hardware complexity and thus the energy consumption and the system area needed for their implementation. Standard video/image algorithm approaches do not yield real-time solutions. Many of these algorithms must be rewritten to include real-time approaches connected to hardware. Moreover, high level tasks such as vision need new and radical methods of processing. For that reason new approaches/algorithms have to be investigated.

In this paper initially we introduce a new approach for low level image processing that meets the above three criteria which are: overall system-level power, performance and area and subsequently we describe a hardware implementation of the proposed algorithm on a FPGA.

The proposed approach is called Coordinate Logic Order Statistics (CL-OS) [1] and is based on Coordinate Logic filters (CLF). CLF decompose a k-bit signal into k binary signals that operate in parallel and achieve the desired processing by executing only direct Boolean functions among the binary levels of the given signal. The philosophy of CL functioning is the process in the bit level of the signal rather in the decimal number level. It can be considered as a bottom up process because the whole filter design starts using base 2 arithmetic functions instead of base 10. This feature is very important since it makes CLF ready for "feeding" H/W.

CL-OS filters apply in parallel a Boolean sorting function $\boldsymbol{f}_{\mathrm{CLS}}$ at each binary level of the signal. The result of the above procedure is the Coordinate Logic Sorting CLS, of the original signal. The filters designed using the above method are the Coordinate Logic Order Statistics filters (CL-OS**)** and they constitute a major sub class of CLF. The functionality of CL-OS filters is similar with that of their corresponding Order Statistics, (OS) [2].

CL-OS filters show similar effectiveness with their corresponding OS filters while they have an explicit superior performance (speed) as well as an explicit lower H/W complexity (resources) and lower energy consumption. For that reason all the wealth of filters, techniques, methodologies and modifications that have been developed using OS may be transferred in CL-OS algorithmic framework.

2. Definition of CL-OS filters

Definition of CL-OS filters: We will attempt to define the CL-OS filters by using an arithmetic example.

Let a set S of five 3-bit numbers,

S = {2, 4, 3, 4, 4}, n=5.

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The array T is the binary representation of the elements of S, (binary decomposition of S). By applying in parallel a CL sorting function $\boldsymbol{f_{CLS}}$ at each column of T we obtain the array T_{CLS} which is the Coordinate Logic Sorting (CLS) of the set S, $T_{CLS} = \{0, 0, 4, 6, 7\}$

$$S=\begin{bmatrix}2\\4\\3\\4\\4\end{bmatrix}\rightarrow T=\begin{bmatrix}010\\100\\011\\100\\100\end{bmatrix}\rightarrow f_{CLS}(T)=T_{sorted}=\begin{bmatrix}000\\000\\100\\110\\111\end{bmatrix}\rightarrow T_{CLS}=\begin{bmatrix}0\\0\\4\\6\\7\end{bmatrix}$$

As it can be seen the sorting procedure pulls down all the 1's of each column of the array T.

The output y of a CL-OS filter is defined as a linear combination of the elements of T_{CLS}

$$y=\sum_{i=1}^{n} w_i T_{CLS}(i),\ i=1,2,\ldots,n \tag{1}$$

Where n denotes the population of the filter mask and w_i are weights.

As seen CL-OS filters consider the signal values as unsigned and an-weighted binary sequences without including carry bits or pointers. The above feature make the CL-OS filters extremely fast while reducing explicitly the H/W needed for their implementation, making their overall complexity $\boldsymbol{O}(n)$ absolutely linear depended only on the population n of the filter window. More over using high fan-in threshold logic gates [3] the overall complexity of the CL-OS algorithmic framework may theoretically be reduced in $\boldsymbol{O}(1)$.

3. Applications

CL-OS filters are appropriate and effective for a wide range of low level image processing tasks including denoising, enhancement, edge and feature extraction, morphological processing, zooming, encryption and cellular automata [1], [6]. Because of limited space we will present only one characteristic application with great demand in computational power:

Signal depended CL-OS median for impulse noise removal (SD-CL-OS median)

In the case of CL-OS filters the detection of a noisy pixel (outlier) is accomplished using information from an estimator g described in eq.(3), [1]. Hence using the obtained value of g we detect the high frequency components of the image and replace them with their CL-OS median. The whole procedure is described as follows

$$\begin{aligned} &if\ \ g \geq T_{CLS}(n-t)\ \ OR\ \ g \leq T_{CLS}(1+t)\ \ then\\ &\qquad y = T_{CLS}((n+1)/2)\\ &\qquad else\ \ y = s_1 \end{aligned} \tag{2}$$

$where\ \ t = 0, 1, \ldots, ((n-1)/4)-1,\ \ n$ is an odd number

n is the number of the pixel elements belonging to the filter mask, s_1 is the kernel origin pixel value and

$$g = s_1 + (2s_1 - (T_{CLS}(1) + T_{CLS}(n))) \tag{3}$$

The filter is applied in parallel at each RGB channel while the final result is the composition of the three filtered channels. Fig. 1 shows the results of the application of a t=0, n= 3x3 SD- CL-OS median as well as the results of the application of a corresponding 3x3 SD-OS median [4].

Fig.1. a) Image corrupted with 40% impulse noise, b) application of 3x3 SD-CL-OS median filter, PSNR = 28.02 db, SSIM =0.56, c) application of a 3x3 SD-OS median filter, 28.73 db, SSIM =0.51

4. Implementation

For the implementation of the CL-OS filters, according to the arithmetic example of section 2, a procedure is required to rearrange or count the 1's at each column of the array T. This task can be accomplished in parallel for all columns of T, without dependences between different columns resulting to a simplified hardware architecture.

The core equations of the CL-OS algorithm have been described using VHDL and implemented on a FPGA. The hardware is parametric in terms of mask size and number of bits per pixel. The entire image is assumed to be stored in a data memory block and the data belonging to the defined mask enter to the CL-OS hardware synchronized with a master clock. Two different hardware implementation approaches have been examined. In the first one an array for sorting all data bits is used. As soon as a new data word appears on the input, every bit is checked and if it is '1', it is directly written in the first free position of the output array starting from the bottom. A set of pointers is used to hold the free position for every column of the array. After processing all data words of the mask, the CL-OS sorted array T_{CLS} of the input variables is available for further processing. The operation described above is illustrated in figure 2 for a mask of 5 8-bit words.

The second hardware implementation approach uses as basic cell a specialized adder, which has inputs with different word-length. The first one is a single bit input while the second one as well as the result are 5-bit wide. Thus, it is possible to count the '1's of an input mask with size up to 31 words (pixels). As in the previous case, a master clock synchronizes the system. Every clock cycle each bit of the input word is added to the respective accumulator and after completion of the entire mask the CL-OS median value is calculated with a comparison of the adder values to the half of the mask size. The operation of the this approach is illustrated in figure 3.

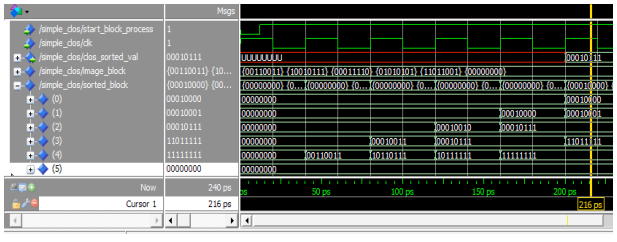

Fig. 2. Simulation results for the first hardware implementation approach

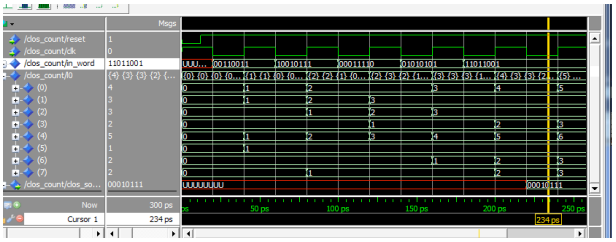

Fig. 3. Simulation results for the second hardware implementation approach.

Hardware resources required for the two alternative implementations of the CLOS core equations on an Altera's Cyclon IV FPGA device are shown in table 1.

Table 1. Hardware complexity of CLOS implementations

MASK SIZE	BIT SORTING		ADDER	
	LEs	REGs	LEs	REGs
3	56	39	48	44
5	104	67	70	59
9 (3x3)	126	84	71	60
15 (3x5)	126	84	65	61
25 (5x5)	180	101	85	61

LE: Logic Element, REG: Register

At this point it is worth mentioning that in both cases we calculate simultaneously all the CL-OS ranks, since a different than the CL-OS median value can be easily obtained by reading a different entry of the output vector containing the sorted values, or by comparing the adders' values to the required rank, respectively.

Comparison results with OS (classic median)

Fig. 4 shows a graph in order to exhibit the H/W performance of the proposed filtering approach against SD-OS median filtering which is a state of the art approach for impulse noise removal. Please note that for the implementation of the SD- OS median a Radix sort [5] algorithm has been used while for the implementation of the SD- CL-OS median our bit sorting algorithm has been used. The first group of curves (indicated with No1) has to do with processing speed while the second group of curves (indicated with No2) has to do with H/W resources. The superiority of CL-OS is obvious.

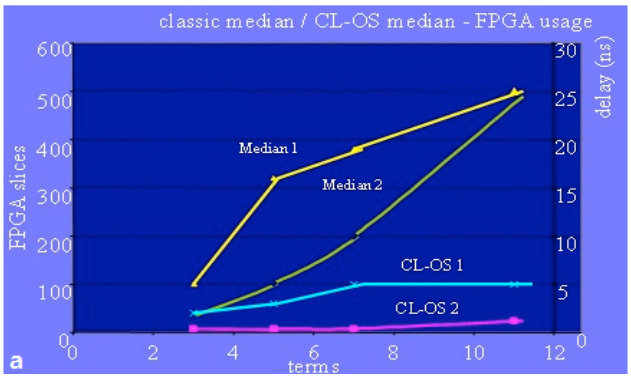

Fig. 4. H/W performance of SD-CLOS median against SD-OS median.

5. Conclusions

A new approach for image/signal processing based on CL-OS filters has been presented. Inherent parallelism, linear complexity, real time performance and efficiency are the main characteristics of CL-OS filters. These features make them appropriate for H/W implementation as well as for real time applications. In the near future, a lot of scientific research may be done, since this new approach opens a new field in order theory and generally in the design of filters using the most minimalistic way. More over the efficiency of CL-OS in various signal processing applications such as speech and voice processing should be investigated as well as their relation with other non linear filters.

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