Jestr

Journal of Engineering Science and Technology Review 9 (6) (2016) 131- 134

Research Article

JOURNAL OF
Engineering Science and Technology Review

www.jestr.org

FPGA-Based Mixed-Signal Circuits Testing System Implementation

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Received 30 September 2015; Accepted 15 September 2016

Abstract

The paper describes the design and implementation of a circuit testing system which has been incorporated into a prototype using FPGAs. The effectiveness of the prototype testing system has been evaluated by applying a test method for analog and digital (mixed-signal) circuits using wavelets and the results are heartening. The operability and efficiency of the system on a technical level is verified in the field. The new fault testing system incorporates reconfigurability and automated input stimulus selection.

*Keywords:*Fault Detection, External Testing System, Mixed-Signal Circuits, Wavelet Transform.

1. Introduction

Although existing test methods for purely digital circuits can cope adequately with the increased complexity, the problem of testing analog – mixed signal circuits, which constitute the majority of modern electronic systems, remains intractable. Existing test methods for mixed-signal circuits and systems have been investigated [1-6] and also have proposed since 1993, for the examination of analog and mixed-signal circuits and the utilization of measurements of the power supply [7-10].

The research team targeted to investigate state of the art technology, providing results, conclusions, comparisons and solutions with respect to the needs of the industry and proposes a method to create new foundations on FPGAs for circuit testing. The mixed signal circuits testing system project managed to develop a test method for mixed-signal electronic circuits and implement the developed method in hardware using FPGA.

2. Design Methodology

The design of the external testing system extracts the signatures of the current from positive, negative and ground power supply lines of the circuit under test (CUT) and then it classifies the CUT accordingly. The methodology used for the good or faulty classification of the CUT derive from the wavelet transformation of the power supply current. The technique is implemented in the testing system.

The power supply current (I_{PS}) of the CUT (positive, negative power supply lines and ground line) is sampled by an external Analog to Digital Converter. Then the data is directed to the FPGA to be processed and to provide the necessary information. Based on the information acquired, a signature database is populated. The database provides the base for comparing the "good" circuits against the measured CUTs for the classification.

The signatures of the referenced circuits and the CUT's are compared with a distance metric. The distance metric is based on the Euclidean distance metric but more effective as an algorithm. The comparison results in a good or fault classification.

Even thought the processing is executed in the FPGA the analog to digital conversion of the current sampling and the digital to analog conversion for the CUT stimulus are executed externally from circuits described in following sections.

The data from the A/D, derived after the sampling, are led to the FPGA. The digital filter in the FPGA, part of the Signal Processing Unit, is used for antiallising and denoising purposes. The next stage of the signal processing unit executes the spectral analysis of the I_{PS} signature using a Fast Fourier Transformation (FFT) and a Discrete Wavelet Transformation (DWT) algorithm to extract the energy of the signature. The unit additionally calculate the rms and mean values of the I_{PS}.

The Digital Stimulus Pattern Generator located inside the FPGA is using the advantage of the FPGA's reconfigurabiltiy based on measurements. The generator applies the correct signal (digital or analog) to the CUT according to the specifications of the CUT. If a circuit cannot be classified from a specific stimulus, then the pattern generator reconfigurability creates a new stimulus that provides a new signature for comparison. This stimulus is created by LUT's, DDS and LFSR. The stimulus can be user selectable, depending on the CUT.

At the end, the decision and classification unit process the data acquired and the calculated signature is compared to the data base signatures of the "good" circuits for the good/fault classification.

3. Testing System Hardware Implementation

The design is embedded into the Virtex-5LXT FPGA from Xilinx. The Development Board (XUPV5-LX110T) features the Virtex-5 FPGA along with a variety of peripherals but also memory elements such as DDR's and Flash Memories. The FPGA itself has 680 I/O pins which can be configured

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in a vast majority of operation modes among with a powerful Clock Management System for zero clock delay and jitter filtering. Moreover, up to 36kb of Block RAM/FIFO's can be incorporated. [11]

The hardware designs implemented are described in the following paragraphs.

The Current Sensing scheme in Fig 1, incorporates a bidirectional Precision Current Sensing Amplifier, the LMP8603 IC from Texas Instruments. The measurement scales for each channel work independently. The output signal is level shifted in order to enable bidirectional current sensing which provides positive and negative values for the current measurements. Accurate measurements are possible, due to the high and common mode voltage inputs (-22 to 60V), in both high and low side current sensing circuit configurations. The output signal is level shifted to meet the voltage input requirements of the ADC.

Operational amplifiers in inverting and non inverting configurations provide the essential voltage measurement stages (positive and negative) and shift the inputs from ±15V to 1.5V and to 3.5V

The DAC circuit provides the input waveforms to stimulate the CUT. The TLV5619 form Texas Instruments is a 12bit DAC with parallel data interface. The 12 bits of data are double buffered so that the output can be updated asynchronously.

The FPGA can provide many different waveforms as input to the DAC which are synthesized in the FPGA.

The last stage buffering before the CUT is regulated by the voltage output amplifier stage in Fig. 2 with the use of the OPA552 from Texas Instruments.

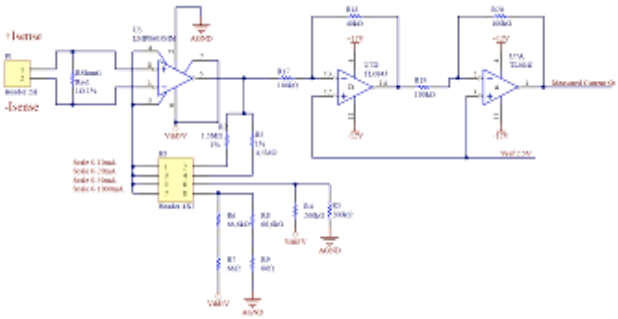

Fig. 1. Current Sensor Unit

The OPA552 is a low noise, high current operational amplifier, with a high slew rate and bandwidth that can sink up to 200mA in continuous mode and its wide voltage output swing with the on chip current limiter can drive the CUT's inputs in any mode of operation safely.

The THS1206 ADC model is used for the conversion of the measurements and provides the external reference voltages needed for the level shifting of the analog signals. Four analog inputs, simultaneously sampled, provide accurate measurements with no time delays. It also provides the external reference voltages for the level shifting of the analog signals from the Current and Voltage measurements sub-circuits (from 0-5V - 1.5V and up to 3.5V) which is the ADC's analog voltage input range.

The power supply of four subsystems provides the power supply voltages (+3.3V, +5V, +12V, -12V) of the board.

The system provides as outputs, the digitally synthesized inside the FPGA waveforms, in its raw digital form. Three level translators are used to provide TTL, 5V-CMOS, 12V-CMOS compatible outputs.

A photograph of the finally constructed testing system is shown in Fig. 3.

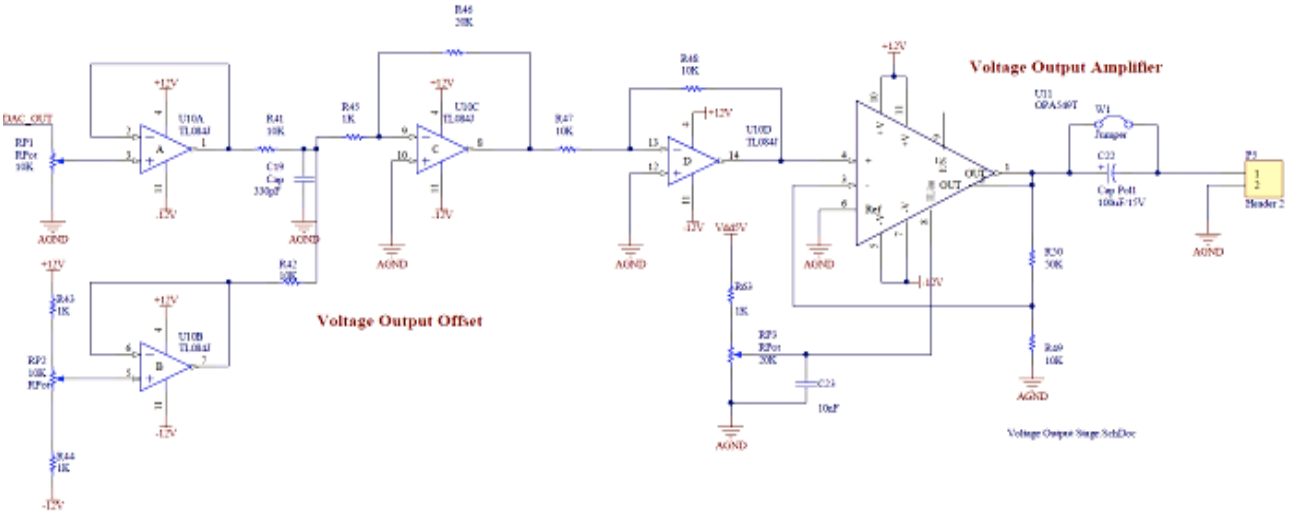

Fig. 2. Voltage Output Offset and Voltage output Amplifier Schematics

4. Testing System Software Description

As mentioned before the system is embedded into the Virtex-5LXT FPGA from Xilinx. The FPGA is populating onto the XUPV5-LX110T Development Board from Xilinx [11].

The software used is Microsoft Windows 7 Professional 64bit Edition, Matlab 2011b incorporating Simulink 6.5 with the DSP 6.5 Toolbox and the Xilinx System Generator for DSP 13.2. The Xilinx ISE 13.2 edition is installed.

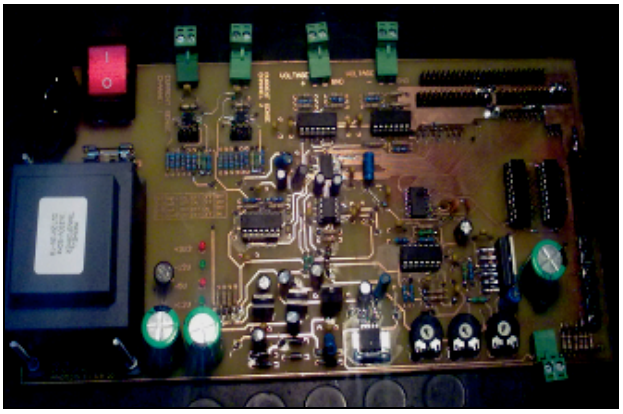

Fig. 3. The Implemented Testing System

A large number of subroutines are developed to account for the multiple requirements such as: interface routines for controlling the keyboard and LCD, storage of the results into the RAM, display of the results, service of interrupt requests, communication routines, routines to perform read/write accesses to the SD memory card. In order to provide a testing system general and applicable to various circuits, the testing scheme is developed in a structural format.

A testing algorithm may be considered as a sequence of elementary steps where measurements and assertions take place. In every step, a quantity (voltage or current) from the CUT is measured and its validity is asserted according to certain user-defined specifications.

For the proposed testing structure, a set of basic procedures (steps) are formed where each one of them is encoded separately and saved as a subroutine in the EEPROM memory.

Three IP cores are used for the development of the system. The Xilinx FIR Compiler 5.0 and the Xilinx FFT 7.1 are part of the Xilinx System Generator for DSP Toolbox and an IP Core is developed incorporating the wavelet transformation for the extraction and calculation of the respective signature of the CUT.

5. Experimental Results

The implemented FPGA-based system is utilized for testing two different circuits [12-15]. The first CUT is the representative operational amplifier circuit in an inverter configuration. The circuit have been implemented using discrete components, where opens are implemented by a resistor of 10 MOhm and shorts by a resistor of 10Ohm. As a second CUT a two-stage MOS amplifier circuit in inverting configuration is used. The circuit consists of a dual power supply (-5V, +5V), 8 MOS transistors, one capacitor and three resistors.

With the presented FPGA-based testing system, the input stimulus signals are dynamically selected and applied as Vin, from a range of three different input stimulus, using appropriately the dynamic stimulus unit. The waveform inputs are: a sinusoidal, a pulse and a triangular, at the same frequency of 1KHz with an amplitude of 0.5V and 50mV respectively. From a set of n=50 known fault-free circuits, the positive I_{PS+}, the negative I_{PS-} and the load current I_L waveforms are measured in the first CUT. Although, in the second CUT the measurements are: the positive (I_{VDD}), the negative (I_{VSS}) power supply current waveform and the load current I_L waveforms. Additional measurements have been taken to improve detectability, like the Vout waveform and the Vrms and mean values.

The results show that the non-linear (pulse or triangular) input stimulus always gives larger fault detectability values than the linear sinusoidal signals. Moreover, the load current I_L waveform always offers greater fault detection ability than the positive and negative current measurement signals [13].

6. Conclusions

A new testing system has been designed and implemented. The system has been used for various CUTs, the emerged results indicate higher detectability values than other existing methods and they have already been presented and published [12-15].

The most important characteristic of the system is that it can be easily reconfigured to test various mixed signal circuits depending on the needs of the industry and it has the capability of automated input stimulus selection.

Work is under way to exploit other testing methods using the implemented FPGA-based testing system, as well as to apply the presented system for testing other complex mixed-signal circuits.

This paper was presented at Pan-Hellenic Conference on Electronics and Telecommunications - PACET, that took place May 8-9 2015, at Ioannina Greece.

Acknowledgements

This research has been co-financed by the European Union (European Social Fund – ESF) and Greek national funds through the Operational Program "Education and Lifelong Learning" of the National Strategic Reference Framework (NSRF) - Research Funding Program: ARCHIMEDES III. Investing in knowledge society through the European Social Fund).

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