Jestr

Journal of Engineering Science and Technology Review 9 (5) (2016) 51 - 55

JOURNAL OF
Engineering Science and Technology Review

Research Article

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Design and Implementation of an Open Image Processing System based on NIOS II and Altera DE2-70 Board

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Received 30 June 2015; Accepted 25 January 2016

Abstract

This paper presents the design and implementation of an image processing system which is based on the NIOS II soft-core embedded processor of Altera. The proposed system which has an open architecture, stands as a useful and flexible platform for the implementation and testing of customized image processing algorithms in hardware. This system is implemented on the FPGA (Field Programmable Gate Array) of the Altera's DE2-70 development platform utilizing the features of Quartus II SoPC (System on a Programmable Chip) builder. It undertakes the real-time processing of images which are either captured by the Terasic's TRDB-D5M camera or they are loaded on system's memory through the available SD (Secure Data) card during the system initialization. The user through the Terasic's TRDB-LTM LCD (Liquid Crystal Display) touch panel controls the operation of the proposed system and observes the results of the selected image processing algorithm.

Keywords: Embedded image processing system; SoPC builder; NIOS II soft-core processor; Cyclone II EP2C70 FPGA.

1. Introduction

Embedded image processing systems are usually appeared in the form of smart cameras and they are used in a wide range of applications in several industries such as consumer, medicine, automotive, robotics, military etc. These systems are equipped with high resolution CCD (Charge Coupled Device) or CMOS (Complementary Metal Oxide Semiconductor) image sensors and they are based on ASICs (Application Specific Integrated Circuits), FPGAs (Field Programmable Gate Arrays) and DSPs (Digital Signal Processors) or combinations of them.

The above systems support simple or advanced image processing algorithms which include object tracking, pattern recognition, face recognition etc. In many cases these algorithms are implemented as hardware components in FPGAs due to the fact that the hardware image processing algorithms could be faster than the corresponding algorithms in C/C++ [1-5].

The aim of this paper is to present the design and implementation of an open image processing system which is based on the NIOS II soft-core embedded processor of Altera [6]. The proposed system is designed with the Quartus II SoPC (System on a Programmable Chip) builder and it is implemented on the Altera's Cyclone II EP2C70 FPGA of the DE2-70 development platform [7-10]. It also utilizes a set of external peripheral devices which include a SD (Secure Data) card, the 5 Megapixel TRDB-D5M camera and the 4.3" TRDB-LTM LCD (Liquid Crystal Display) touch panel by Terasic [11, 12].

The advantage of the proposed system is that the user is able with minor modifications to integrate her/his own image processing algorithms which are developed in HDL (Hardware Description Language) utilizing the features of the Quartus II SoPC builder. For demonstration purposes the proposed system integrates 4 simple image processing algorithms, including negative colour, sobel edge detection, median filter and sharpen convolution filter. These 4 algorithms have been designed and implemented, except one, as hardware blocks in VHDL (VHSIC - Very High Speed Integrated Circuit HDL).

2. System Overview

The architecture of the proposed system is presented in Fig.1 and it consists of three main sub-systems and a number of ready IP (Intellectual Property) cores [13-14]. The Camera sub-system is responsible to initialize the TRDB-D5M camera and to manage the captured image frames. The Image Processing sub-system processes the current image by applying the selected hardware image processing algorithm. Finally, the Touch Panel sub-system undertakes the initialization and the operation of the TRDB-LTM LCD touch panel.

Through the JTAG Uart core, the user is able to download and debug the program in C/C++ which is executed by the NIOS II soft-processor utilizing the features of the NIOS II SBT (Software Build Tools) for Eclipse IDE (Integrated Development Environment) [15]. At this point it is worth to be mentioned that the NIOS II soft-processor undertakes the control of the system's hardware components and it is not responsible for the implementation of the supported image processing algorithms.

During the system initialization procedure, the data of three bitmap images which are previously stored in the SD card by the user, are transferred to the system's SDRAM (Synchronous Dynamic RAM - Random Access Memory) through the SD Card Controller and the SDRAM Controller cores. The proposed system is able to process either the static images which are stored in the SDRAM or image

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frames which are captured by the TRDB-D5M camera according to the selected operation mode (Video or Photo Mode).

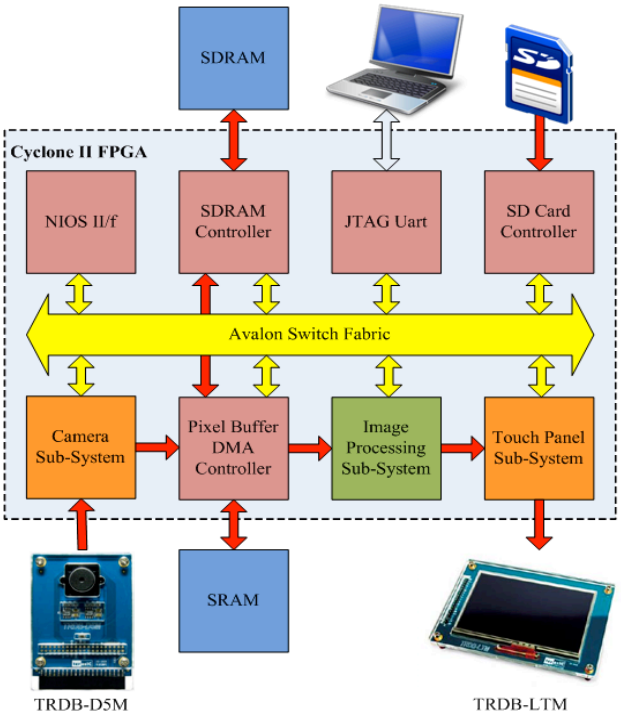

Fig. 1. The block diagram of the open image processing system.

In the Video Mode operation which is the default operation mode, the captured by the TRDB-D5M camera image frame is transferred to the Pixel Buffer DMA Controller core through the Camera sub-system. The Pixel Buffer DMA Controller core temporarily stores the current image frame in the system's SRAM (Static RAM).

When the system switches from the Video Mode to the Photo Mode operation the current image frame which is previously stored to the system's SRAM is also stored to the system's SDRAM by the Pixel Buffer DMA Controller and the SDRAM Controller cores. According to user's choices the selected image is transferred by the SDRAM Controller core to the Pixel Buffer DMA Controller core which temporarily stores the selected image in the system's SRAM.

In both operation modes the Pixel Buffer DMA Controller core transfers the image which is stored in the system's SRAM, to the Image Processing sub-system. The Image Processing sub-system applies the selected image processing algorithm to the initial image and transfers the processed image to the Touch Panel sub-system in order to be displayed in the TRDB-LTM LCD touch panel.

The hardware implementation of the proposed system is loaded to the Cyclone II EP2C70 FPGA of the DE2-70 development platform. The total implementation takes up to 18% of the 68,416 logic elements, 0% of the 8626 registers, 22% of the 1,152,000 memory bits, 3% of the 300 9-bit embedded multipliers and 25% of the 4 PLLs (Phase Locked loops). Consequently, the above FPGA has enough free space for the implementation of more complex hardware image processing algorithms.

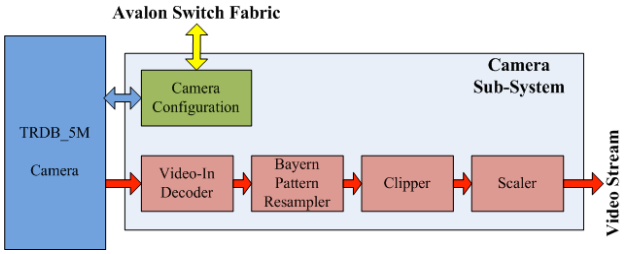

Fig. 2. The block diagram of the Camera sub-system.

3. Camera Sub-System

The Camera sub-system which is presented in Fig.2 is responsible to capture image frames from the TRDB-D5M camera.

During the system initialization procedure the Camera sub-system undertakes the configuration of the TRDB-D5M camera through the Camera Configuration core. This core is able to access anyone of the 256 registers of the TRDB-D5M camera through the I2C (Inter Integrated Circuit) interface in order to control the parameters of the available image sensor. The selected parameters are transferred to the Camera Configuration core by the NIOS II soft-processor through the Avalon Switch Fabric [16].

According to the block diagram of Fig.2 the Camera sub-system captures the current image frame from the TRDB-D5M camera using the Video-In Decoder core. The captured image frame which has a resolution of 2592x1944 pixels, is converted by the Bayern Pattern Resampler core from the Bayern format to the 24-bit RGB format with the half resolution (1296x972 pixels). The resolution of the captured image frame should be reduced to 640x480 in order to be compatible with the specifications of the TRDB-LTM LCD touch panel. This task is achieved by the Clipper and Scaler cores of the Camera sub-system. The Clipper core removes from the incoming image 8 columns from the right and the left sides and 6 rows from the top and the bottom. As a result the resolution of the image frame is reduced to 1280x960 pixels. The final reduction of the image frame resolution is achieved by the Scaler core which is configured with 0.5 scaling factors for both the width and height. Consequently, the captured image frames which come out from the Camera sub-system, are in 24-bit RGB format with a resolution of 640x480 pixels.

4. Image Processing Sub-System

The Image Processing sub-system which is presented in Fig. 3, applies the selected hardware image processing algorithm, to the incoming image. It is worth to be mentioned that the images should be in 24-bit RGB format with a resolution of 640x480 pixels.

The selection of the desired hardware image processing algorithm is transferred to the PIO (Parallel I/O – Input/ Output) core by the NIOS II soft-processor through the Avalon Switch Fabric. The PIO core controls the Video Stream Router core which operates as a demultiplexer (Split Mode) and transfers the incoming image to the selected image processing core. The processed image comes out from the Image Processing sub-system through the Video Stream Router which operates as a multiplexer (Merge Mode).

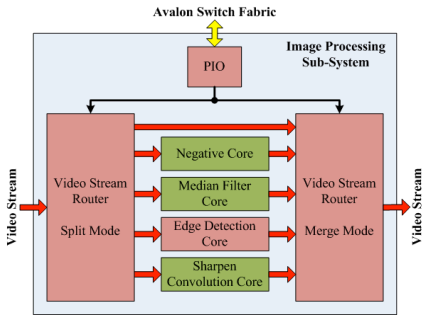

Fig. 3. The block diagram of the Image Processing sub-system.

The proposed system for demonstration purposes supports 4 image processing algorithms which are implemented by the Negative, Median Filter, Edge Detection and Sharpen Convolution cores. Besides the Edge Detection core which belongs to the UP (University Program) IP Library of Altera, the other 3 cores have been designed and developed from scratch in VHDL utilizing the features of Quartus II IDE and the SoPC builder [8, 9].

This fact confirms that the proposed system supports either custom image processing cores developed by the user or ready image processing cores from the UP IP Library. The advantage of the proposed system is that the user is able to integrate her/his custom cores in order to verify the implemented image processing algorithms by replacing the corresponding cores of the Image Processing Sub-System without any further modifications.

5. Touch Panel Sub-System

The Touch Panel sub-system which is presented in Fig.4 is responsible for the operation the TRDB-LTM LCD touch panel.

During the system initialization the Touch Panel Configuration core configures the parameters of the TRDB-LTM LCD touch panel. These parameters are sent to the above core by the NIOS II soft-processor through the Avalon Switch Fabric. In addition, the Touch Panel Configuration core reads from the available ADC (Analog to Digital Converter) the x-y coordinates of the activated area every time the user touches the TRDB-LTM LCD touch panel. Subsequently, the Touch Panel Configuration core transfers the x-y coordinates to the NIOS II soft-processor through the Avalon Switch Fabric.

The incoming image should be converted to 30-bit RGB format with a resolution of 800x400 pixels according to the specifications of the selected touch panel. This task is accomplished by the RGB Resampler and the Clipper cores. The RGB Resampler core undertakes to convert the incoming image from the 24-bit RGB format to the 30-bit RGB format. The Clipper core adds to the incoming image 80 black columns to both sides. As a result the total image resolution is increased to 800x400 pixels and two black areas are displayed in both sides of the incoming image.

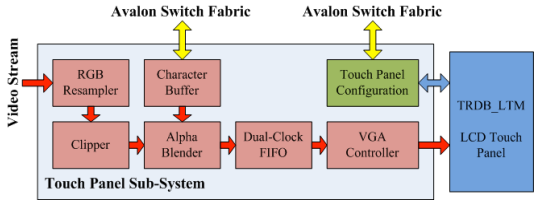

Fig. 4. The block diagram of the Touch Panel Sub-System.

These areas will be used for the creation of the virtual buttons in order to control the system's operation.

The text of the virtual buttons and the corresponding coordinates are sent to the Character Buffer core by the NIOS II soft-processor during the system initialization. The Character Buffer core converts the ASCII characters of the above text into their graphical representation with a resolution of 50x30 pixels per character and it sends them to the Alpha Blender core.

The Alpha Blender core combines the incoming image with the graphical representation of the virtual buttons' text from Character Buffer core. The final image is transferred to the Dual-Clock FIFO (First In First Out) core. This core is responsible for the synchronization of clock signals between the incoming image frames and the VGA Controller core. The VGA Controller core generates the required timing signals for the TRDB-LTM LCD touch panel. Through this procedure both the processed image and the text of the virtual buttons are displayed in the TRDB-LTM LCD touch panel.

6. System Operation

As it was mentioned above the total operation of the proposed system is controlled by the NIOS II soft-processor. The program (Fig.5) which is executed by the NIOS II soft-processor, is developed in C/C++ utilizing the features of the NIOS II SBT (Software Build Tools) for Eclipse IDE.

During the system initialization procedure the NIOS II soft-processor loads to the SDRAM the three bitmap images with a resolution of 640x480 pixels which were pre-stored in the available SD card by the user. Subsequently, it initializes the TRDB-D5M camera and the TRDB-LTM LCD touch panel through the corresponding sub-systems and selects the default operation mode which is the Video Mode.

When the system initialization is completed the user is able to control the system operation through the virtual buttons of the TRDB-LTM LCD touch panel. Due to this, the NIOS II soft-processor checks periodically if a virtual button is pressed through the x-y coordinates which are sent by the Touch Panel sub-system.

The NIOS II soft-processor changes the system operation mode if the virtual buttons "Video" or "Photo" are pressed. When the Photo Mode operation is selected the NIOS II soft-processor before change the operation mode, stores the current image frame to the system's SDRAM. According to this scenario the SDRAM of the DE2-70 board contains the data of 4 images in 24-bit RGB format with a resolution of 640x480 pixels.

The user is able to select the one of the available image processing algorithms by enabling the corresponding image processing core through the appropriate virtual button. She/he is able to disable all the image processing cores through the virtual button "Normal" in order to observe the original image frame or the stored image according to the selected operation mode.

If the Photo Mode operation is selected, the user through the virtual buttons "Previous" and "Next" is able to select one of the stored images.

7. Examples

In the presented examples, the user has already stored in the SD card 3 bitmap images files in RGB format with a

resolution of 640x480 pixels. The data of these images are loaded to the system's SDRAM memory during the initialization procedure. In the first example the selected image is processed by the negative colour core according to user's choices. The result image (Fig. 6) is displayed in the TRDB-LTM LCD touch panel and the user is able to observe the results of the selected algorithm. In the second example the selected image is processed by the edge detection core and the result image (Fig. 7) is displayed in the TRDB-LTM LCD touch panel.

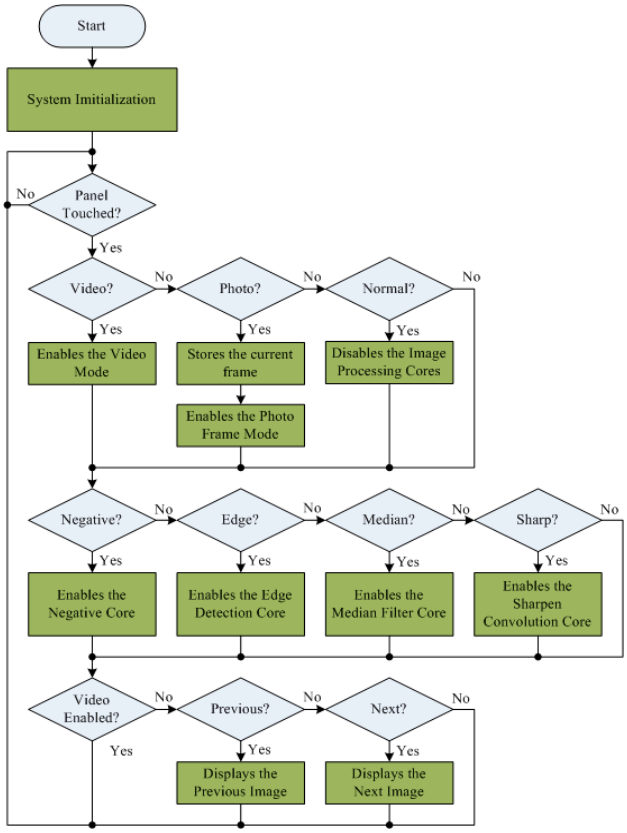

Fig. 5. The block diagram of the NIOS II program.

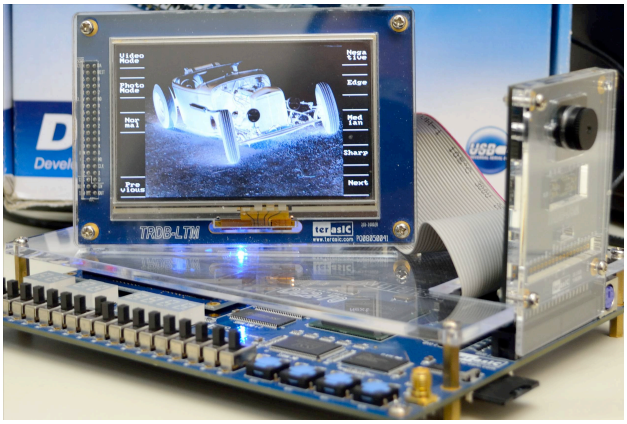

Fig. 6. The result image of the negative colour algorithm.

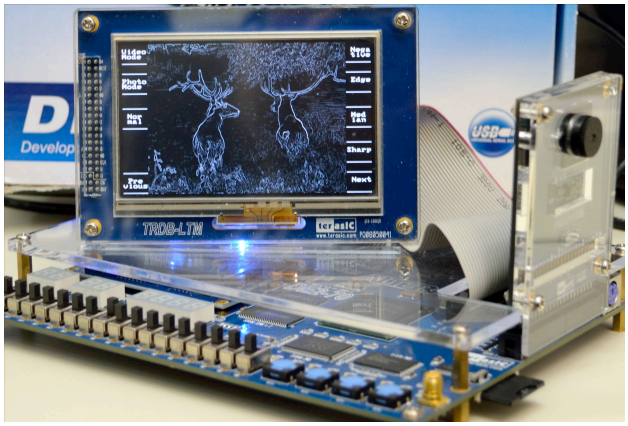

Fig. 7. The result image of the edge detection algorithm.

8. Conclusions

This paper presents an open image processing system based on the NIOS II soft-processor which is implemented on the DE2-70 development platform of Altera. The proposed system processes images which either are captured by the available TRDB-D5M camera or were pre-stored by the user in a SD card. The user is able to observe the processed image and to control the operation of the system through the virtual buttons of the TRDB-LTM LCD touch panel.

For demonstration purposes the presented system supports 4 hardware image processing algorithms which include the negative colour, the edge detection, the median filter and the sharpen convolution filter. Besides the edge detection algorithm, all the other image processing algorithms are developed as hardware components in VHDL utilizing the features of the Quartus II IDE and the SoPC Builder.

The great advantage of the proposed system is that the user is able to verify the operation of custom hardware image processing algorithms simply modifying the Image Processing sub-system. This fact, allows the proposed system to be used as a platform for implementing and testing customized image processing algorithms in hardware.

Future plans include the extension of the proposed system's features in order to allow the user to manage the image files which are pre-stored in the available SD card and to select the desired image file through a user friendly menu. In addition, the user will be able to save either image frames or the processed images in the SD card as image files. The integration of an Ethernet controller in the proposed system seems to be a challenge because it will allow the remote control of the proposed system. According to this scenario the user will be able to remotely control the proposed system and to observe the results of the selected image processing algorithm through a personal computer or a mobile device.

This paper was presented at Pan-Hellenic Conference on Electronics and Telecommunications - PACET, that took place May 8-9 2015, at Ioannina Greece.

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