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CeidMem: A compact Static Memory Library

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Abstract

In this paper the implementation of a compact static memory library, called CeidMem, is presented. The library is based on the UMC technology and the 65nm low leakage process. The library is complete having basic memory cells, sense amplifiers, read/write circuitry and data bus precharge units. Moreover memory circuits are presented and their structure is explained. In conclusion, a complete example design which uses CeidMem as in chip level one cache, is analysed and simulated in order to confirm the correct functionality and behaviour of the library.

Keywords: SRAM; static RAM; cache; memory library; layout; VLSI.

1. Introduction

The implementation of a whole chip, besides the pads, includes not only the function of the core circuitry which is mainly implemented as an intra-network connection of a set of standard cells, but also the in-chip memory circuitry. This memory circuitry, in most cases, is implemented to act as level one cache and uses the same technology process of the standard cells that implement the core of the chip. This led our academic institute (CEID), having recently implemented a standard cell library [1] to also implement a memory library for the support of academic projects that include complete integrated circuit design. Both libraries use the same umc 65nm low leakage technology process [4], making them compatible and therefore capable of being presented inside the same die.

2. The Memory Library

The memory library is complete including the basic 6T memory cell used to create the memory storage grid and also prechargers, sense amplifiers and read-write multiplexers [2]. Besides these basic cells, other supporting cells are inserted to the library. The supporting cells are divided in the row and the column ones, and are mainly used as predecoders and as wire line extenders. Most of the memory library cells, with a brief explanation of their behaviour, are presented on Table I.

2.1. CeidMem 6T Memory Cell

The main storage element of the CeidMem library is the 6T memory cell. This cell is designed to support auto vertical and horizontal abutment. The vertical abutment auto expands the memory bit lines and the horizontal abutment auto expands the address. The library's 6T memory cell and moreover the abutment of the cell is presented at figure 1.

Table 1. Memory Library Cells

Cell Name	*Cell Behavior*
MC6TTYP	Typical 6T memory model
MCAMPCCA	PCCA type sense amplifier
MCRWMUX	Read – Write multiplexer
MCWAMP	Write amplifier
MCWENAMP	Write amplifier with enable
MCBLPREEQ	Precharger with Equalizer
MCBLPREBEQ	Neg precharger with Equalizer
MCD6TTYP	Double 6T memory cell
MCBLTG	Bit line transmission gate
MCBLTGMRY	Alternate layout for bit line transmission gate
MCBUFCX1	Column buffer
MCBUFENCX1	Tristate column buffer
MCBUFRX1	Row buffer
MCINVCX1	Column inverter
MCINVRX1	Row inverter
MCNOR2X1_RMC	2 to 1 Nor gate adjacent to the memory cells row. Used for address predecoding
MCNOR2X1_RRDC	2 to 1 Nor gate adjacent to the sense amplifier row. Used for sector read predecoding
MCNOR2X1_RWRC	2 to 1 Nor gate adjacent to the write amplifier row. Used for sector write predecoding
FILLR_MC6TTYP	Filler cell for memory cell row
FILLR_MCAMPCCA	Filler cell for sense amplifier row
FILLR_MCBLPREEQ	Filler cell precharger row
FILLR_MCWENAMP	Filler cell write amplifier row
MEM16X16	16x16 non-interleaved static ram example
MEM256X8X4	1Kx8 interleaved static ram example

Both the n-type and the p-type transistors, support a channel width of 150nm. This is the minimum channel width to support a perfect alignment between the PMOS and the NMOS circuitry resulting to a total height of 1.62um and a total width of 1.34um giving an area of 2.1708um^2 per memory Cell. The 6T memory cell is also provided with a metal 3 route through that is mainly used to extend the address signals towards the predecoded memory sectors.

2.2. CeidMem Read – Write Circuitry Cells

The amplifier chosen to support the read function of the memory is the PMOS cross-coupled [3]. Main advantage of this amplifier is its fast sense speed. The layout implementation and the functional response of the sense

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amplifier used by CeidMem, is presented at figure 2 (a). The sense amplifier is triggered when a positive pulse is issued at its SAen metal 3 input. As a result, the metal 2 BL and BLB memory value is sensed and the outputs are set at the metal 4 Dout and DBout signals. The write functionality of the CeidMem library is supported by the amplifier illustrated in figure 2 (b). The write amplifier is triggered by its enable metal 1 WEN input and via inverters connected in series, the input data sets or resets the memory's data lines. The functional response of the CeidMem's read –write circuitry is presented at figure 2 (c).

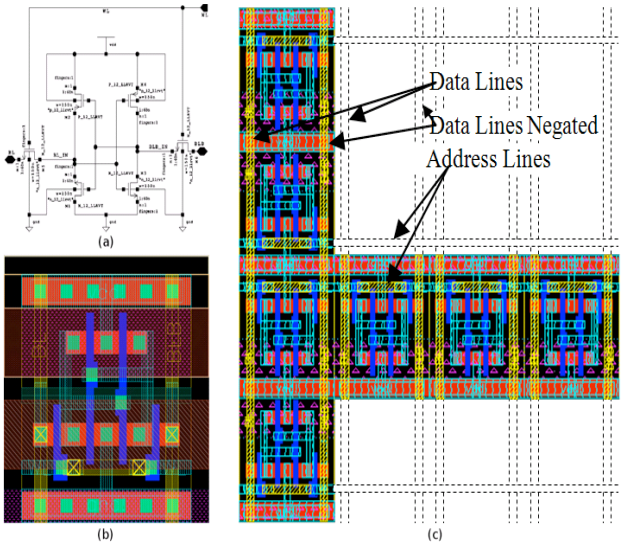


Fig. 1. 6T memory cell (a) schematic view (b) layout view (c) abutment

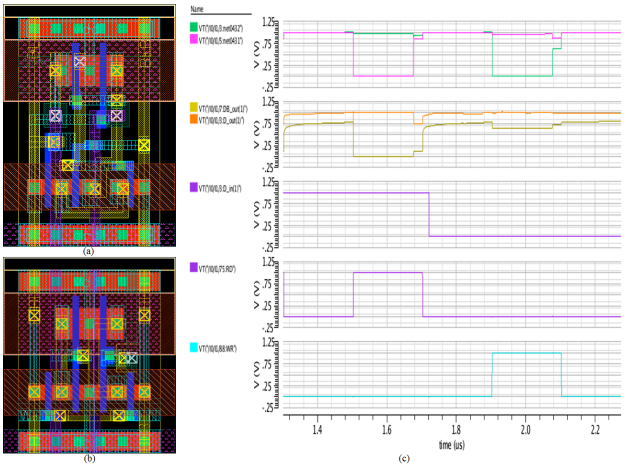


Fig. 2. (a) PCCA Layout (b) Write amp Layout (c) Read –Write functionality

3. The Compact Memory Grid Structure

In order to make the library the compact possible, all library cells, that implement the memory grid [3], support special route through lines which help the address signals and the read-write signals to propagate without the need of the use of extra line tubes. The memory structure is illustrated in figure 3.

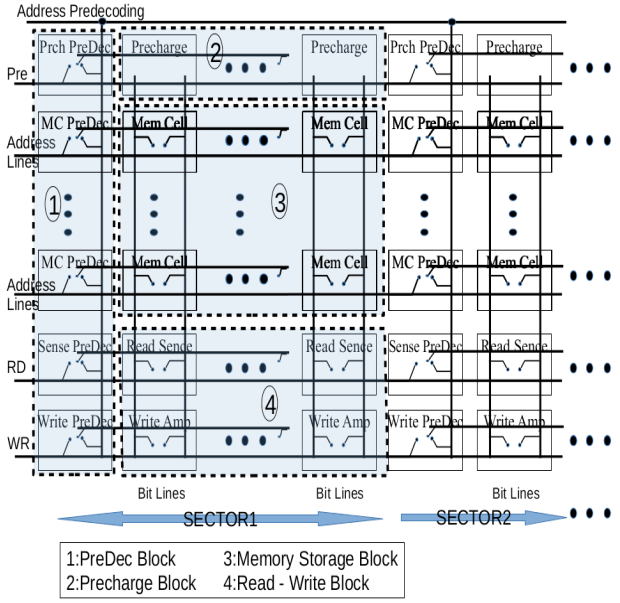


Fig. 3. CeidMem generic grid structure

The PreDec memory block is used as the first memory block when memory interleaving is needed. Using the PreDec modules the address, the precharge and the memory read-write signals are propagated only at the activated memory sector. Having the PreDec block immediate adjacent to the storage block is a technic that amplifies the compact characteristics of CeidMem memory structure. The connection of the MC PreDec unit with the memory storage cells is presented at figure 4. The connections of the other PreDec units are done in a similar and corresponding way.

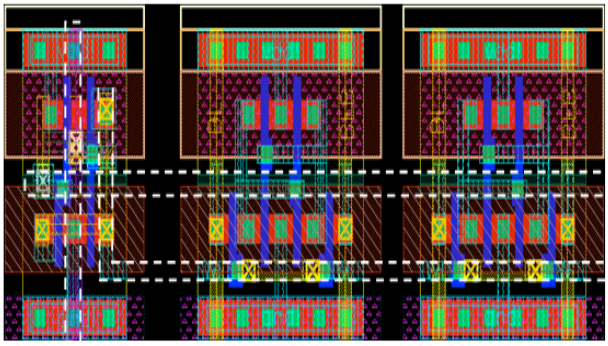


Fig. 4. Address line predecoding and data line extension

Moreover, to support bigger memory designs memory row and column inverters and buffers are inserted to the library to act mainly as data line extenders.

3.1. CeidMem Grid Area Estimation and Calculation

Due to the compact layout of the CeidMem library, the portion of the area that is used by the PreDec block the Precharge block and the Read – Write Block is insignificant compared to the area needed by the memory storage block. So the estimated area that is needed for the complete memory circuitry inside the chip die is

$$CeidMemEArea = 0.94 * memcells * 2.1708um^2 \quad (1)$$

However, if a more accurate area estimation of the implemented memory is needed, taking into account the

other special memory blocks, then the precise memory area is

$$CeidMemPArea = \begin{cases} memcells * 2.1708um^2 \\ +overhead \\ +overlapping \end{cases} \quad (2)$$

Overhead stands for the additional area needed by the PreDec, the Precharge and the Read-Write memory blocks and is defined as

$$overhead = \begin{cases} num\_PreDec * 1.8144um^2 \\ +num\_Precharge * 3.16um^2 \\ +num\_ReadWrite * 6.6744um^2 \end{cases} \quad (3)$$

As memories grow in size, the area occupied by the memory cells is quite bigger compared to the area that is characterized as overhead. So the increase rate of the memory cells area is quite bigger than the increase rate of the overhead area, leading to the equation

$$\lim_{memArea \to \infty} \frac{overhead}{memArea} = 0 \quad (4)$$

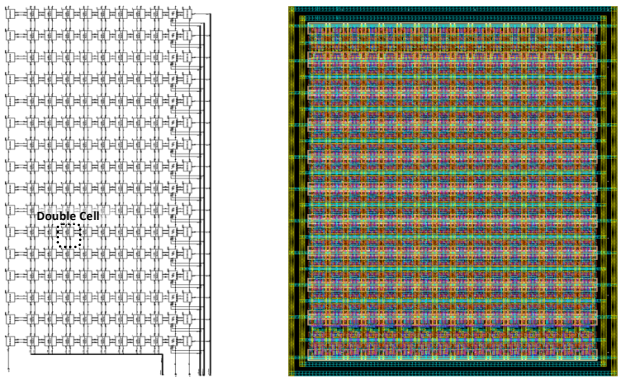
Overlapping is defined as the area mostly used by the power and the ground rails. This particular area is overlapped as cell abutment develops and is calculated by the equation

$$overlapping = memArea * 6\% \quad (5)$$

4. CeidMem Examples

4.1. 16x16 non-interleaved memory grid example

A simple memory implementation, without interleaving, is presented at figure 5. Each memory storage cell is a double cell fitting exactly one bit of data for two consecutive address locations, resulting to a memory of size 16 locations, occupying 16 bits each. This is the actual static memory design used for the verifications of the proper operation of the CeidMem's storage cells.

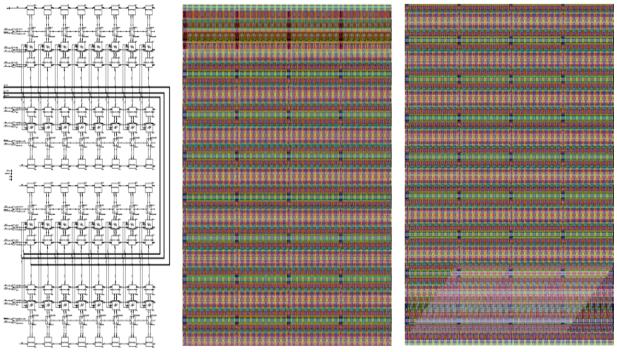


Estimated Area: 522,38um²
Excact Area: 555,52um²

Fig. 5. 16x16 Memory

4.2. 1Kx8 memory grid example interleaved to 4 sectors

A more advanced memory implementation, that uses interleaving, is presented at figure 6. This design describes a static memory using most of the cells provided with CeidMem library. The memory is divided to four sectors with the address predecoding technique. Each sector holds 256 memory locations each of which can store 8 bit of data. So, for example, altering the third address signal, the memory location 255 x PreDec + 3 is activated to read or write data. Making the memory sector enabled using interleaving, the portion of the memory that is operative is minimized and hence the memory power consumption is minimized too.



Estimated Area: 16716,20um²
Excact Area: 17006,64um²

Fig. 6. 1Kx8 Memory

The 16x16 and the 1kx8 static memory cores are provided with the memory library distribution.

5. Verification Of The Memory Library

The correct operation of the CeidMem memory library is verified using cadence integrated environment [5] and confirmed by sequentially storing and reading values at it. Moreover, the compatibility with the Ceid Standard Cell Library [1] is checked by reading and writing data via circuitry that is implemented on this standard cell library. The test circuit is presented at figure 7. This test circuit includes the 16x16 static random access memory which is implemented with cells of CeidMem library connected to an addition subtraction core unit. The core unit is synthesized and implemented on Ceid Standard Cell Library [1]. It includes three registers. Two of these registers act as input to the function of the unit. The third, which is a multiplexed one, stores the result of the function which is going to be written to the memory or sends the data immediately to access the memory.

A complete memory circle of operation was provided to the test circuit. So, at the beginning, two data values are stored in the memory. First data 0011d is stored in memory location 1 and data 0110d is stored in memory location 2. An addition function is called at the core and the output 1001d is stored in memory location 9. Then memory location 9 is read and the output data bus showed the correct value. The signals of the memory interface are presented at figure 8.

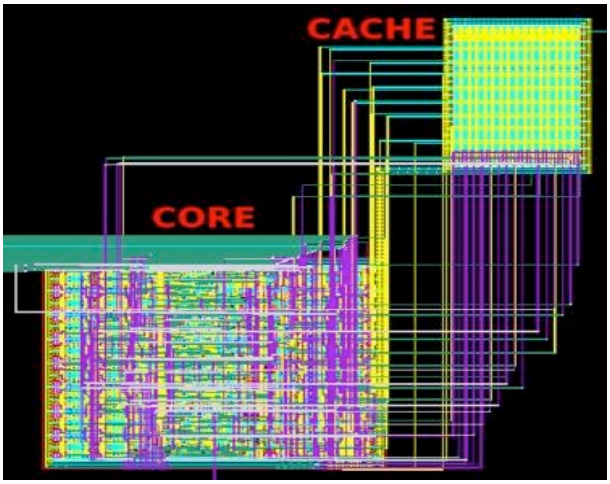


Fig. 7. Memory test circuit

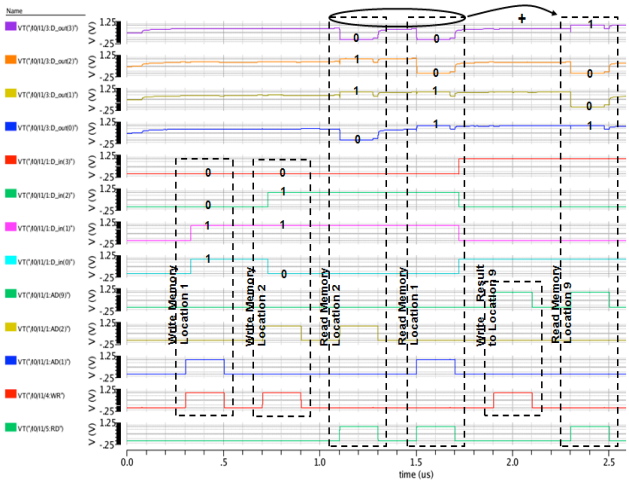


Fig. 8. CeidMem response signals

6. Distribution Of The CeidMem Library

In order to make the CeidMem memory open to the academic community, a website that allows the downloading of the complete version of the library has been created. The website can be reached at the address https://www.ceid.upatras.gr/webpages/courses/vlsilab/index_en.html

7. Future Work

The implementation of a tool, like a memory compiler, will take place. The tool will be coded on cadence skill language [5] and the automated extraction of static memories will be possible with it, using cells from CeidMem library. Also the configuration of different interleaving memory schemes will be allowed and the communication with the compatible Ceid Standard Cell Library [1] will be simplified as the extracted memory blocks will be able to be automatically inserted and connected to the core blocks. Moreover the target of the CeidMem library is to achieve low power applications due to the materials it is implemented on, so a low power memory analysis, characterization and estimation will be exported via the tool.

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