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Delay Elements Suitable for CMOS Ring Oscillators

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Abstract

This work presents a survey of state-of-the-art delay elements, which are suitable for high-frequency pseudo-differential CMOS ring oscillators. Also, it proposes a novel delay element, which is based on two CMOS inverters loaded by a simple pMOS negative resistance. The delay element is employed to the construction of a 3GHz 4-stage ring oscillator. The ring oscillator performance is designed in order to be compliant with the MIPI Alliance M-PHY standard, which is the most updated high-speed serial interface technology. The proposed delay element and the ring oscillator are simulated with 65nm CMOS process with a supply voltage of 1.2V featuring -94dBc/Hz phase noise, 6.4mA current consumption and an almost constant K_{VCO} equal to 5.7GHz/V.

Keywords: High speed serial interfaces, PLL, VCO, CMOS Ring Oscillators, Delay Elements

1. Introduction

During the last decade, many traditional high-speed circuit designs like voltage controlled oscillators (VCOs) which normally use LC tanks tend to be substituted by active CMOS Ring Oscillators (ROs) [1], [2].

The basic block topology of an active CMOS ring oscillator is shown in Fig. 1. The topology is, actually, a closed unstable negative feedback loop which comprises an odd number of identical inverters. The delay element (DE) in the basic topology is actually a simple CMOS inverter. The output waveforms are also shown in Fig. 1 and, eventually, exhibit rail-to-rail voltage swings. Due to the unstable condition, the circuit oscillates with a time delay of T_D between two consecutive output voltage nodes yielding an oscillation frequency of f_o=1/2N·T_D. The time delay depends on (a) the current drive capability of the inverters and (b) the parasitic capacitance C_{par} of the output nodes. The time delay and, therefore, f_o can be tuned from the voltage supply V_{DD}, since through V_{DD} the current drive strength can be easily adjusted. So, V_{DD} is normally the frequency tuning voltage V_{CTRL} of the RO as it is shown in Fig.1. V_{DD} is the internal power supply of the RO and not the supply of the entire system.

The basic performance features which characterize the efficiency of ring oscillators are the following: (a) wide tuning range in order to compensate the process, temperature and power supply (PVT) variations, (b) low power consumption, (c) low phase noise (d) low voltage supply operation capability, (e) high output voltage swing (f) common-mode signal rejection and (g) duty cycle equal to 50%.

The topology of Fig. 1 which is the single-ended version of a RO, suffers from poor power-supply noise rejection ratio (PSRR) and, generally, from poor common-mode rejection ratio (CMRR). The differential topology counterpart, which is shown in Fig. 2a, presents better CMRR performance and is, probably, the best candidate for low voltage supply environment. Also, the differential implementation can utilize an even number of stages by simply configuring one stage such that it does not invert.

The block diagram of the differential DE, which is employed in many differential RO topologies and, perhaps, is the most suitable solution, is presented in Fig. 2b. It is constructed by a transconductance input stage (g_m) which drives the parasitic capacitance C_{par} of the output stage, the output conductance g_o of the input stage and the negative conductance g. The negative conductance along with C_{par} and g_o defines the oscillation frequency. Assuming that the small signal circuit approximation is valid [5], the oscillation frequency is given by

$$f_o = \frac{\sqrt{g_m^2 - (g_o - g)^2}}{2\pi C_{par}} \quad (1)$$

Fully differential g_m structures as they are presented in Fig. 2c present high CMRR but unfortunately are not suitable for low supply voltage applications, because of the necessary voltage headroom needed by the tail current source. Therefore, the pseudo-differential g_m stages, as they are shown in Fig. 2d, are the best candidate for such applications. The absence of tail current produces higher output voltage amplitudes, but on the other hand degrades the CMRR. To improve CMRR, the usage of negative conductance is necessary since it rejects the common-mode signals. Due to the negative conductance, the CMRR is given by

$$CMRR \approx \left[(g_o + g)/(g_o - g)\right] \quad (2)$$

From eq.(2), it is obvious that as the value of the negative conductance is close to the output conductance, the CMRR becomes high.

This work studies the utilization of a differential DE in a 4-stage CMOS RO. The RO performance is designed to be

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compliant with MIPI Alliance M-PHY specification - the most updated industrial standard that defines the link for high-speed short range wire-line applications [3].

In section II, the specification overview of the MIPI Alliance MPHY standard is analyzed. In section III, an overview of suitable DEs for low supply voltage ROs is presented. In the same section a novel DE which is based on simple CMOS inverters is described. In section IV the simulation results of the proposed DE are presented.

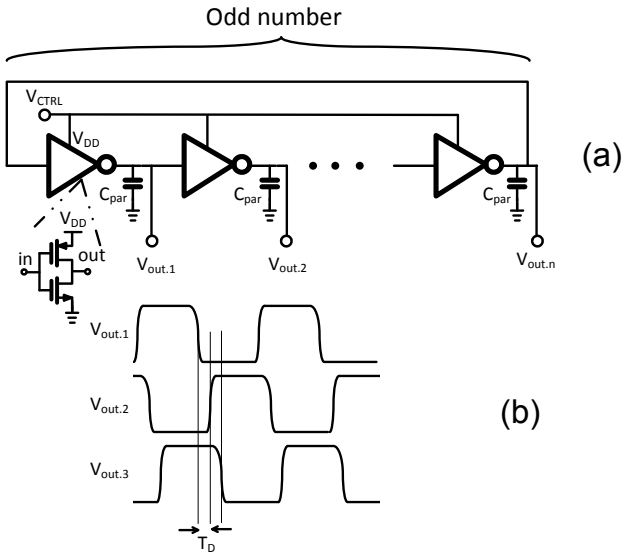

Fig. 1. (a) RO basic single ended topology with CMOS inverter based delay element and (b) output waveforms

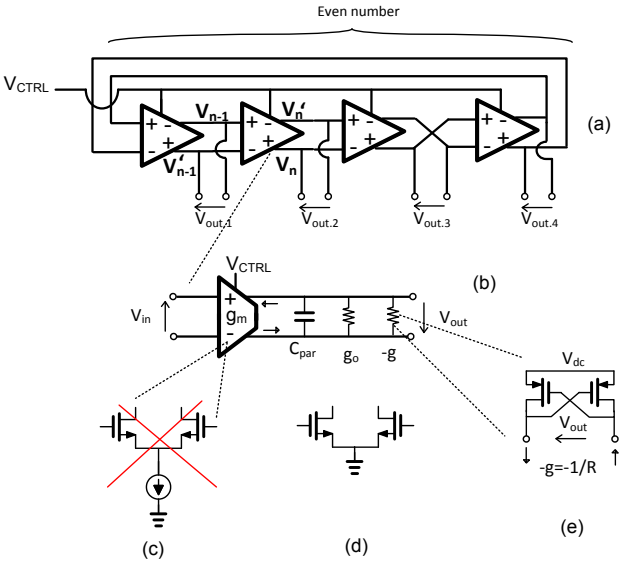

Fig. 2. (a) Differential RO (b) block diagram of delay element (c) fully differential gm stage (d) pseudo-differential gm stage and (e) basic structure of active differential negative conductance -*g*.

2. M-PHY Standard and RO system specification

The MIPI Alliance M-PHY specification is the most updated industrial standard that defines the link technology for high-speed short range wire-line applications [3]. The M-PHY specification is developed for mobile applications providing high bandwidth capabilities with very good power efficiency. Its serial interface contains a transmitter (TX) and receiver (RX) which communicate with each other via high-speed differential signalling.

The M-PHY specification supports three discrete high-speed gears (HS1/2/3) and two data rates per high-speed gear (rate A/B). Assuming that the clock and data recovery system of the RX uses a half-rate binary phase detector, the oscillation frequencies required by the RO are $f_{HS1A/B}$=0.624/0.7288GHz, $f_{HS2A/B}$=1.248/1.4576GHz and $f_{HS3A/B}$= 2.496/2.9152GHz which correspond to HS1, HS2 and HS3, respectively. TABLE I presents the RO specification in order to be compliant with the MPHY standard.

Table 1. RO specifications compliant with M-PHY standard's HS3

S/N	Characteristic	Symbol	Units	Value
1	Supply Voltage	V_{DD}	V	1.2
2	Current consumption	I_{DD}	mA	≤8
3	Tuning Voltage Range	ΔV_{TUNE}	V	0.2 - 1
4	Oscillation Frequency	*fHS3.A*	GHz	2.496
5	Oscillation Frequency	*fHS3.B*	GHz	2.9152
6	Phase Noise @ 1MHz	pn	dBc/Hz	≤-92

3. Delay elements overview

3.1. DE with controllable latch

The circuit diagram of the DE which employs a CMOS latch is illustrated in Fig. 3 [4]. Transistors M_{p1+}-M_{p1-} form a pair of pMOS latches which implements a positive feedback loop that ensures oscillation. The intensity of the latch is controlled by the nMOS transistors M_{i+}-M_{i-} through the their gate voltage which act as the control voltage V_{CTRL}. As V_{CTRL} decreases, the latch gain loses its intensity resulting in lower oscillation frequency. The main drawback of this element is that the input-output response experiences a dead zone resulting in a duty-cycle different than 50%.

3.2. DE with controllable current source

The circuit of this DE is shown in Fig. 4 [5]. It consists of the nMOS input pair M_{n1+} and M_{n1-}, the pMOS negative conductance formed by M_{p1+}-M_{p1-}, the diode-connected PMOS pair M_{p2+}-M_{p2-}, and the pMOS tail transistor M_B for frequency tuning. The frequency tuning is achieved by tuning the transconductance of M_{p2} by controlling the current of the tail transistor M_{b1}. The current of M_B is controlled through its gate voltage V_{CTRL}. Since g_m is a non-linear function the drain current, the f_o-V_{CTRL} relationship will feature a non-linear relationship. Due to the last, the loop dynamic of a PLL that uses a RO with this DE will be affected.

3.3. DE with controllable current-starved inverters

The DE which is based on a balanced current-starved inverter structure, M_{n1+}/M_{p2+} and M_{n1-}/M_{p2-}, is shown in Fig. 5 [6]. The frequency tuning is achieved using the current starving technique, which has been implemented using the control current I_{CTRL}. Moreover, this topology has additional pMOS transistors M_{ADD}, which are connected to the output nodes and, directly, connected to the supply voltage. These transistors offer higher output voltage swing, but need extra circuitry (e.g. voltage regulator) to reduce the high sensitivity on the supply voltage variations.

3.4. DE with active inductors

This DE is presented in Fig. 6 and employs active inductors in order to tune the parasitic capacitances adjusting in this

manner T_D [1]. Active inductors present some advantages compared with the passive inductors, such as reduction in die area and low substrate noise coupling, but present higher noise due to active device noise contribution and poor quality factor Q. The active inductors are realized by nMOS active loads M_{L+}–M_{L-} and the controllable pMOS resistors M_{g1}-M_{g2} which are biased in the triode region. By controlling the resistance of M_{g1}-M_{g2} through V_{CTRL}, the delay time constant is $\tau_{del}= R_{eff}C_{eff}$ where

$$R_{eff} = R_S(V_{ctrl}) + \omega^2 \frac{L_S^2(V_{ctrl})}{R_S(V_{ctrl})} \quad (3)$$

$$C_{eff} = C_L - \frac{L_S(V_{ctrl})}{R_S^2(V_{ctrl}) + \omega^2 L_S^2(V_{ctrl})} \quad (4)$$

3.5. Proposed DE with CMOS inverters

The proposed DE is shown in Fig. 7 and it is constructed by two CMOS inverters $M_{n1+/-}$-$M_{p2+/-}$ and a negative conductance formed by a pMOS transistor pair M_{p1+}-M_{p1-}. The frequency tuning is achieved through the supply voltage $V_{DD.RO}$ of the RO which acts as the control voltage V_{CTRL}. Including the proposed DE into a RO we achieve an oscillation frequency which is actually proportional to V_{CTRL}.

The frequency tuning is achieved without using current starving as in [6]. The current through M_{p2+}-M_{p2-} which charges the parasitic capacitance of the output nodes follows the changes of the V_{CTRL}. Therefore, the time delay and the oscillation frequency can be tuned through V_{CTRL}.

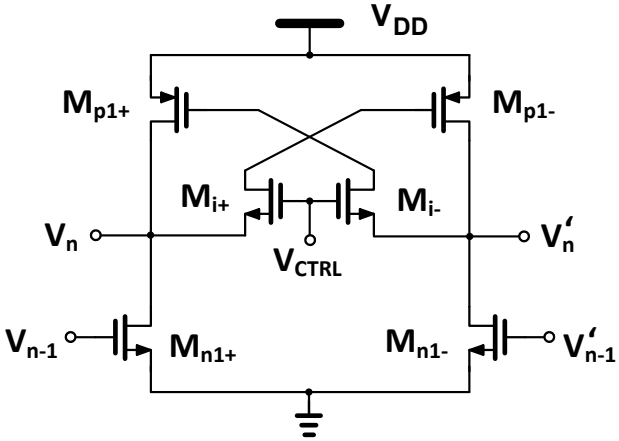

Fig. 3. Delay element with controllable latch

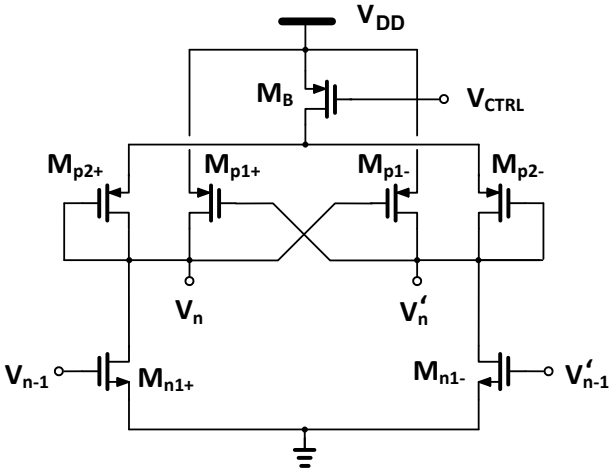

Fig. 4. Delay element with controllable current source

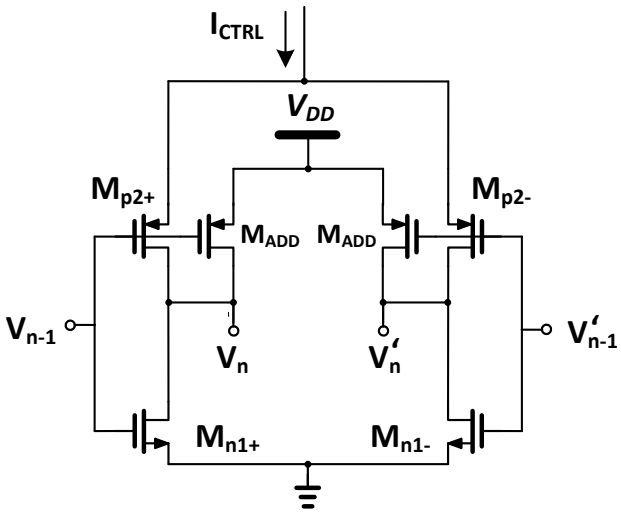

Fig. 5. Delay element with controllable current-starved inverters

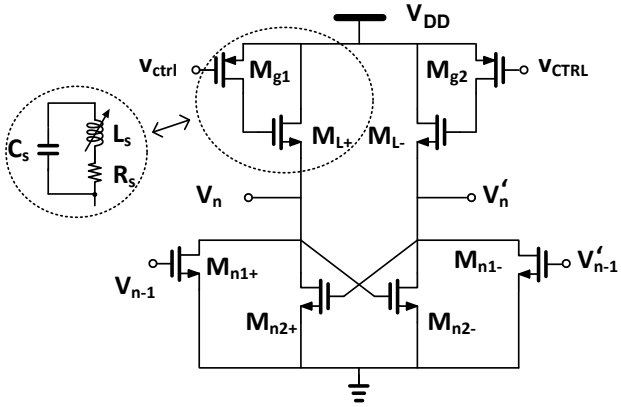

Fig. 6. Delay element with active inductors

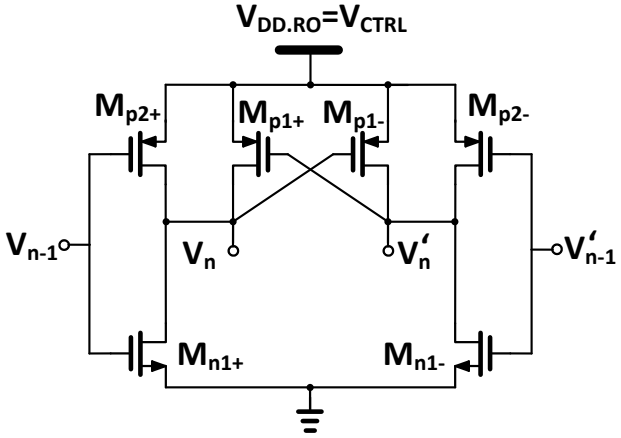

Fig. 7. Proposed delay element with CMOS inverters

4. Simulation results

All simulations were performed with the Spectre simulator of the Analog Design Environment of Cadence software. The proposed DE is designed and simulated in a 65nm CMOS process.

The proposed DE of Fig. 7 is included in a 4-stage RO similar with that in Fig. 2a and its overall performance is verified. It should be mentioned here that the complete RO should include several necessary circuitries such as level shifters, common-mode stabilizers and output buffers.

Also, a voltage regulator is employed in order to drive all DE with the appropriate current which is necessary to keep the oscillation conditions. In addition, the voltage regulator actually converts tuning voltage which it normally comes from the charge pump of the PLL into the appropriate frequency control voltage V_{CTRL}.

As it is shown in Fig. 7, the output voltage swing will not be constant, but it is limited by V_{CTRL} because it is the supply voltage of the DE. The level shifter amplifies the output amplitude of the RO and makes it equal to the voltage supply of the entire chip. The common-mode stabilizer regulates the common mode level of the output waveforms achieving in this manner 50% duty cycle. Finally, the output buffers are required in order to drive the next stage and isolate the RO.

Table II presents the performance of a 4-stage RO which is consisted of the proposed DE and includes all aforementioned necessary circuitries.

Fig. 8 illustrates the oscillation frequency as a function of V_{CTRL} concerning the rates A/B of HS3. The control voltage V_{CTRL} ranges between 0.6-0.9V. The K_{VCO} is constant and the f-V_{CTRL} characteristic is linear. The last is very important because it ensures stability of the loop dynamic of PLL that uses a VCO with the proposed DE as building block. In Fig. 9, the phase noise performance of the RO versus the offset frequency from the carrier is presented.

Table 2. Performance of RO optimized for HS3/Rate B: $f_{HS3.B}$ = 2.915GHz

S/N	Characteristic	Symbol	Units	Value
1	Supply Voltage	V_{DD}	V	1.2
2	Current consumption	I_{DD}	mA	6.4
3	Tuning Voltage Range	ΔV_{TUNE}	V	0.6 - 0.9
4	Linear Frequency Range	Δf_{LINEAR}	GHz	1.9
5	(Frequency/Voltage) Gain	K_{VCO}	GHz/V	5.7
6	Phase Noise @ 1MHz	pn	dBc/Hz	-94

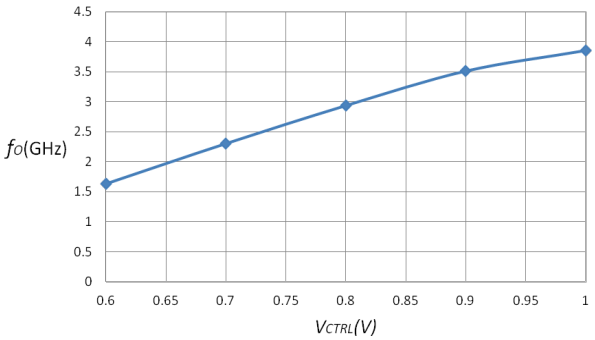

Fig. 8. Simulated oscillation frequency versus V_{CTRL}

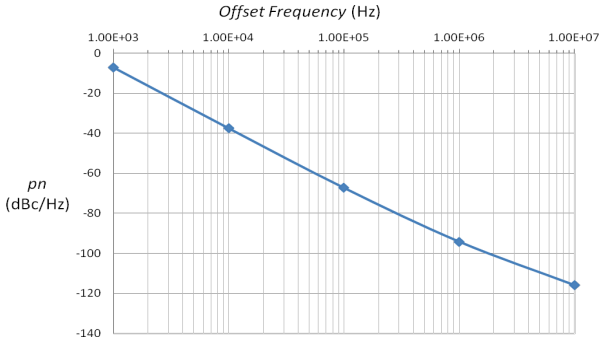

Fig. 9. Phase noise versus offset frequency

5. Conclusion

This work presents an overview of existing delay cells suitable for the implementation of a CMOS RO, along with a proposed DE which is constructed by two CMOS inverters loaded by a negative resistance. The main assets of the proposed DE against its counterparts, is that when used as building block in a RO scheme, the oscillator exhibits a wide tuning range with a constantly linear K_{VCO}. However, extra circuitries are needed to ensure rail-to-rail output voltage swing. Finally, simulation results indicate that the proposed DE can be used in a RO that it is compliant with the M-PHY standard.

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