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A Configurable Design for Morphological Erosion and Dilation Operations in Image Processing using Quantum-dot Cellular Automata

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Abstract

This paper presents a novel configurable design for the implementation of basic morphological operations based on Quantum-dot Cellular Automata (QCA) technology. QCA is a promising technology in the field of nanoelectronics that could be utilized in many image processing applications. QCA architecture will provide better performance by exploiting parallel processing, better silicon-area utilization, maximization of clock speed and very low power consumption. Fundamentals of QCA technology and circuit design and the basic operations of mathematical morphology are presented in brief. A new innovative QCA design that is capable to implement either the erosion or the dilation morphological operation, configured by the value of one-bit input is designed, simulated and tested with success.

Keywords: quantum cellular automata, QCA design, nanoelectronics, image processing, mathematical morphology.

1. Introduction

Nowadays, the size of electronic devices continues to decrease towards the nanometer scale. But, there are certain physical limitations that restrict the ability of greater reduction such as the power consumption, the interconnectivity and lithography problems. Nanoelectronic circuits are expected to replace the CMOS circuits in the near future. There are several emerging nanoelectronic technologies, which have been proposed by researchers during the last years. Silicon nanowires, carbon nanotubes, single-electron transistors (SETs) and circuits, Quantum-dot Cellular Automata, resonant tunneling diodes, and single-molecule devices are some of the most promising emerging technologies which are reported by ITRS [1]. The QCA technology and its computational scheme uses highly pipelined architectures and extremely high speeds. It does not use electric current flow to codify the information, but the positions of electrical charges in the interior of the QCA cells. So, an efficient design of circuits based on QCA technology would lead to the reduction of both the computational complexity and power consumption. Therefore, QCA is considered as one of the most promising emerging nanoelectronic technologies [2, 3, 4, 5].

By using QCA technology, the integration can reach densities of 1012 cells/cm^2 and the circuit switching frequency can be close to terahertz [1]. Although, the main advantages of QCA designs are the improvement that offer in size, speed and power consumption, there are also some other characteristics that give advantage to QCA technology, such as the ability to cross wires in a plane [5] and a new computation and information representation method which is referred to as processing-in-wire [2]. Therefore, QCA is a new opportunity for innovative designs such as: an automated QCA design architecture for 1-D Cellular Automata [6], a QCA T flip-flop [7], a QCA design of a 5-input majority gate [8], a serial communication system using QCA [9], a modular 2n to 1 multiplexer [10] and a modular multiplexer for memory accessing [11].

Most of image and video processing algorithms are very demanding in speed and computational power. VLSI technology that was extensively used in the past, have been proven a reliable solution for improving the performance of image and video processing systems. Some examples of successful implementations include nonlinear filters [12], multi-functional image processing applications [13], video noise reduction [14] and non-linear image processing operations [15]. In many of hardware implemented image processing systems, mathematical morphology operations are used as parts of more complicated image processing algorithms.

Recently, some interesting QCA designs have been proposed for image processing applications, such as morphological edge detection [16], thresholding [17] and noise removal [18]. In [19] the authors have proposed two efficient but non-configurable QCA designs for morphological erosion and dilation.

In the following section, basic concepts of mathematical morphology will be presented, and a simple description of the quantum-dot cellular automata will follow in Section 3. The configurable QCA design of the morphological erosion and dilation operations will be presented and simulated in Section 4 and conclusions will be drawn in Section 5.

2. Mathematical Morphology

Digital image and video applications are present almost everywhere in our daily lives. But, there are cases where the quality of digital images and videos reduces to unsatisfactory levels. Common reasons for low quality are the unconstrained camera motion, the uncontrolled indoor or

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outdoor environments, the existence of clutter and the exposure to noise during signal transmission. Although there are many algorithms proposed in the literature trying to improve the quality of corrupted images, only few are easily implemented in hardware. Mathematical morphology algorithms have the advantage to give easy hardware implementations and therefore are extensively used as parts of more complex algorithms.

Mathematical morphology is a field of image processing that offers theoretical foundation and powerful tools used in several image and video processing applications [20, 21, 22]. Some of the basic algorithms are used for thinning, thickening, skeletonising, shape extraction, segmentation, object detection and tracking, noise reduction, feature point selection, face recognition and verification and many more [23, 24, 25, 26]. There are also some more complex morphological algorithms such as interpolation of 3D binary objects [27], robust 2D and 3D object representation [28].

The basic operations of mathematical morphology are erosion and dilation. They take two sets of data as input: the input image and the structuring element. The simpler version of mathematical morphology is applied on binary images (with only black or white pixels) and uses binary structuring elements. It will be assumed that in binary images, white pixels represent background regions, while black pixels denote foreground, although in some implementations this convention is reversed.

To compute a mathematical operation on a binary image using a structuring element, each of the pixels in the input image (usually called input pixel) should be considered in turn. For each pixel, we superimpose the structuring element over the input image, so that the origin of the structuring element (usually the central pixel) coincides with the input pixel position. The set operator applied on the image pixels values and taking into account the structuring element pixels values gradually produce the output image.

The erosion morphological operation is presented in the following. As it is shown in Fig.1, suppose A is a binary object in the input image and S is a structuring element (only the black pixels). We denote $S(i,j)$ the S placed with its origin pixel at a certain pixel (i,j) of the input image. The erosion of A by S is defined to be the set of all pixel locations for which S placed at that pixel is contained in A. This is denoted $A \ominus S$ and is written as:

$$A \ominus S = \{(i,j): S(i,j) \subset A\} \qquad (1)$$

Fig.1 presents the input image with the binary object A, the structuring element S which is a 3×3 cross and the eroded image $A \ominus S$ where the grey pixels are the eroded pixels that are subtracted from the object (in fact they are white).

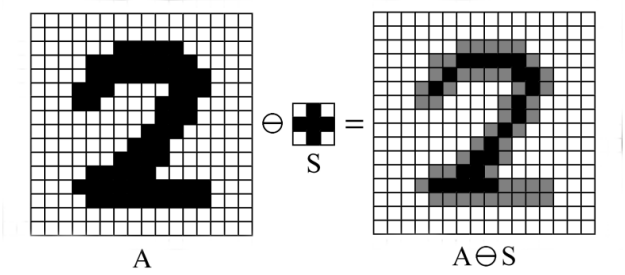

Fig. 1. The erosion of an object by a structuring element

Dilation can be defined as a complementary to the erosion operation, but an alternative definition that helps to understand how it is applied is the following. Let as assume that S' is the reflection of S. Obviously, S' equals S for symmetrical structuring elements. Then the dilation $A \oplus S$ contains all the pixels lying in any $S'(i,j)$ for which $(i,j) \in A$. So, the dilation is the union of the pixels, of a copy of S' at every pixel of the binary object A in the input image. This definition is written as:

$$A \oplus S = \bigcup_{(i,j)\in A} S'(i,j) \qquad (2)$$

Fig.2 presents the object A in an input image, the same structuring element S which is symmetrical and the dilated image $A \oplus S$ where the grey pixels are the dilated pixels that are considered as part of the output image (in fact they are black).

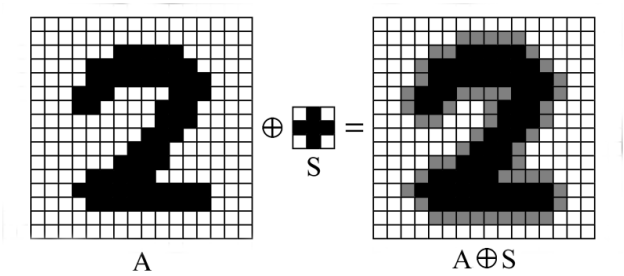

Fig. 2. The dilation of an object by a structuring element

The design and simulation of erosion and dilation with one configurable QCA circuit will be presented in Section 4.

3. Quantum-dot Cellular Automata

In conventional digital technologies the binary values "0" and "1" are represented by ranges of voltage or current. In contrast, QCA uses the position of electrons in quantum dots to represent the binary values. The information is stored as configurations of electron pairs in quantum dot arrays. The unit of information is kept in a QCA cell which is presented in Fig.3. The QCA cell is the basic building block of QCA devices and it consists of four quantum dots in a square array coupled by tunnel barriers. The physical mechanisms for interactions between dots are the Coulomb interactions and quantum-mechanical tunneling. Electrons are able to tunnel between the dots, but cannot leave the cell. If two mobile electrons are placed in the cell, in the ground state and in absence of external electrostatic influence, Coulomb repulsion will force the electrons to dots on opposite corners [2, 3, 4, 5]. The two possible charge configurations are presented in Fig.3 and correspond to binary "0" and "1".

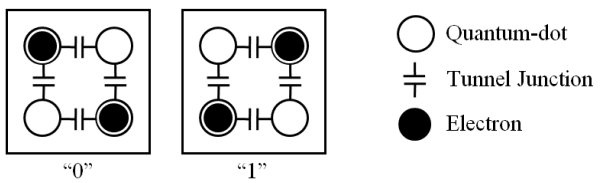

Fig. 3. The two possible charge configurations of a QCA cell

The proper placement of QCA cells leads to the implementation of basic QCA circuit components. For

example, the successive placement of QCA cells one after the other in one direction, acts like a wire and is usually called binary wire [2]. The three-input majority gate is one of the most important processing elements in QCA circuits and its implementation was proposed in [5]. The majority gate is constructed with a cross structure. The logic function of the three-input majority gate is $\mathrm{M(A,B,C)} = \mathrm{AB} + \mathrm{AC} + \mathrm{BC}$ and the output has to be the same as the majority of the three inputs A, B, C. The implementation is composed of five cells as shown in Fig.4. In the example that is presented, $A = 1$, $B = 0$ and $C = 0$. The electrostatic forces between the electrons of the three input cells, constrain the electrons of the centric cell to get the state of logic "0". Generally, the state of the centric cell is set by electrostatic forces from the logic state of the majority of the inputs. This state is then transmitted to the output cell at the right.

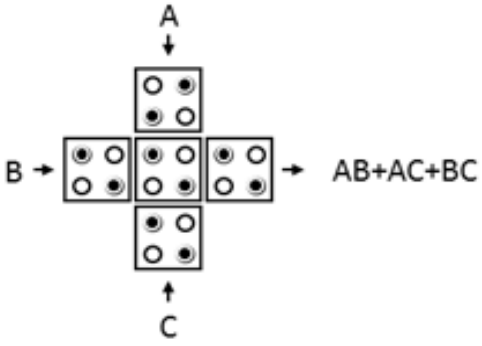

Fig. 4. The majority gate QCA implementation

The AND and OR logic gates can be implemented as special cases of the majority gate. When in a majority gate one of the inputs is steadily set to "0", then this gate operates as the AND gate. When it is steadily set to "1", then this gate operates as the OR gate. Based on this simple observation, it can be considered that when one input of the majority gate is configured as "0" or "1", then the majority gate can act either as an AND or as an OR gate respectively. So, the majority gate can be considered as a configurable AND/OR gate with two inputs A and B and another input "sel" that configures the gate and controls its behaviour, as it is shown in Fig.5. This design has two inputs A and B and the outcome will be either their logic AND, if the third input ("sel") is set to "0" as presented in the figure, or their logic OR, if the third input ("sel") is set to "1". The output is symbolized as AB or $A + B$ respectively.

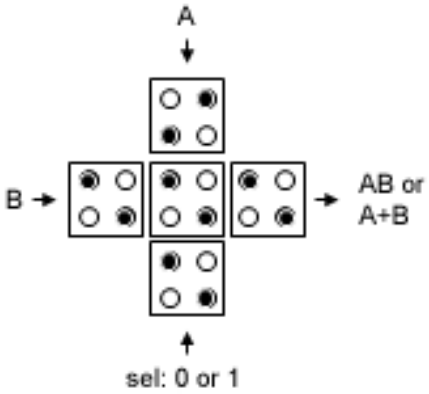

Fig. 5. The configurable AND/OR gate designed using QCA cells

4. Configurable QCA implementation of morphological erosion and dilation

As it was presented in the previous section, the implementations of logic gates using QCA are quite simple. The logic of using the majority gate, and the uniformity of wires and processing elements, modify the way of thinking in designing circuits. In the following, the image processing morphological operations of erosion and dilation, which were described in Section 2, will be implemented by using QCA technology and utilizing the configurable AND/OR gate which was presented in Section 3.

The configurable QCA implementation of morphological erosion/dilation operation, which is proposed, is one single design that can execute either the erosion or the dilation operation configured by one of its inputs. In order to guarantee its functionality, the proposed design keeps the basic rules for a successful design: the wire lengths are less than 10 cells, the length of phase blocks are 2 cells or more and the areas of clocking zones and uncovered areas have been kept as small as possible [29, 30].

The proposed design is presented in Fig.6. It consists of four majority gates which act like configurable AND/OR gates. As it is shown in the figure the "sel" input configures the majority gates. When the "sel" input is set to logic "0" it makes the majority gates to behave as AND gates. When the "sel" input is set to logic "1" it makes the majority gates to behave as OR gates.

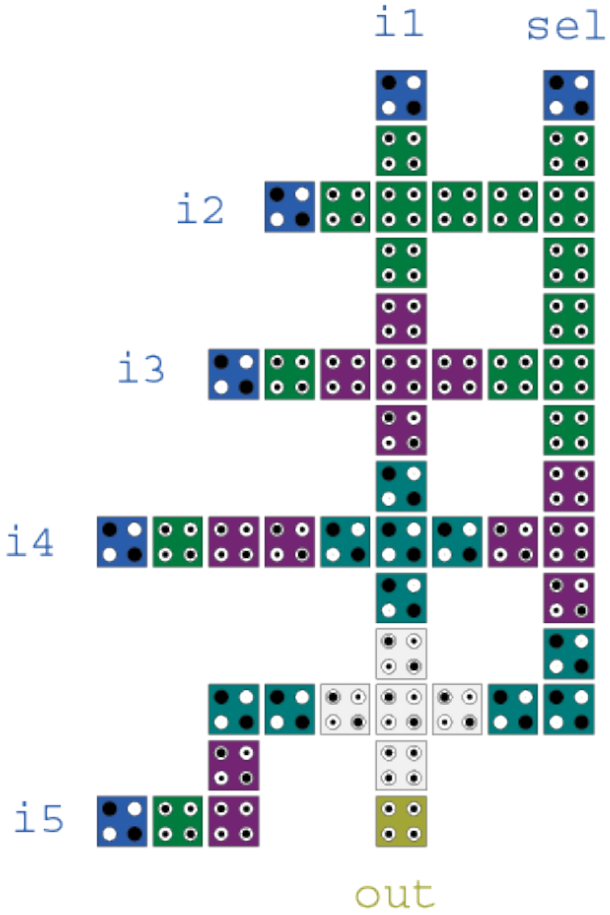

Fig. 6. The configurable QCA circuit for morphological erosion or dilation

For the explanation of the implementation let us assume that black pixels correspond to logic "1" and that white pixels correspond to logic "0". It is also assumed that the

inputs are binary images with white background and black objects and that the structuring element is a 3×3 pixels cross with origin its centric pixel, as they are presented in Fig.1 and 2.

4.1. QCA Implementation of Morphological Erosion

The procedure that applies the morphological erosion can be simplified to the following steps. First, superimpose the structuring element over every 3×3 region of the image. Then, if all the black pixels of the structuring element coincide with black pixels on the input image, paint black the pixel of the output image that corresponds to the structuring element origin. In other cases the pixels of the output image are left white.

This operation can be implemented in hardware by the design presented in Fig.6. The "sel" input is set to logic "0", so the majority gates behave as AND gates. The design implements a 5-input AND gate by the proper connection of four 2-input AND gates. The inputs (i1 to i5) are fed by the values of the five input image pixels that coincide to the five structuring element black pixels.

The output of the 5-input AND gate will be logic "1" only if all the inputs (i1 to i5) are set to logic "1" and the state of the output cell will define the value of the pixel of the output image with coordinates that corresponds to the coordinates of the structuring element origin pixel. So, if all the pixels of the input image (which coincides with the structuring element) are black, then the pixel of the origin on the output image will be black. In other cases, the output will be logic "0", so the output pixel will be white.

This QCA design was simulated and tested with the use of the QCADesigner tool [31]. According to this tool, the design consists of 51 cells covering an area of 178× 278 nm^2 that is approximately 0.05 μm^2. It is covering an area of 9×14 grids and the ratio of the area covered by QCA cells to the overall area of the layout is 0.405.

The first half of Fig.7 presents the simulation results of the QCA morphological erosion operation, which confirms the correctness of the design. As it is shown all possible value combinations of 5 inputs are applied to the circuit. The "sel" input is set to logic "0" which means that the design is configured for erosion operation. The output is set to logic "1" only when all inputs (i1 to i5) stay at logic "1" otherwise is set to logic "0" indicating the AND gate behaviour that leads to a successful morphological erosion operation.

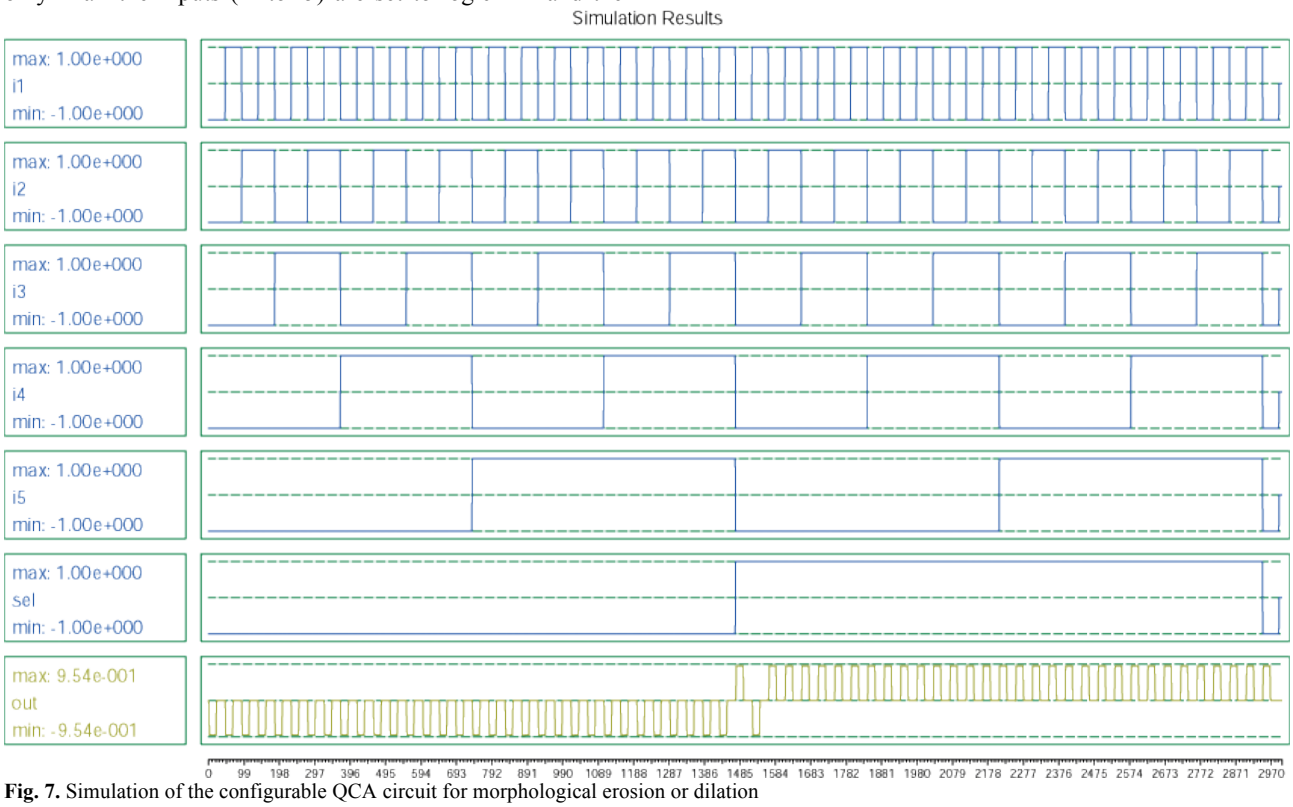

Fig. 7. Simulation of the configurable QCA circuit for morphological erosion or dilation

4.2. QCA Implementation of Morphological Dilation

The QCA implementation of morphological dilation operation will be described in the following. The procedure that applies the dilation can be simplified to the following steps. First, superimpose the structuring element over every 3×3 region of the image. Then, if the black pixels of the structuring element coincide with one or more black pixels on the input image, paint black the pixel of the output image that corresponds to the structuring element origin. In other cases the pixels of the output image are left white.

This operation can also be implemented in hardware by the design presented in Fig.6. The "sel" input is set to logic "1", so the majority gates behave as OR gates. The design implements a 5-input OR gate by the proper connection of four 2-input OR gates. The inputs (i1 to i5) are fed by the values of the five input image pixels that coincide to the five structuring element black pixels.

The output of the 5-input OR gate will be logic "1" if one or more of the inputs (i1 to i5) are set to logic "1". The state of the output cell will define the value of the pixel of the output image with coordinates that corresponds to the coordinates of the structuring element origin pixel. So, if one or more of the pixels of the input image (which coincides with the structuring element) are black, then the pixel of the origin on the output image will be black. On the contrary, when all the inputs have the value of logic "0" the output will be logic "0", so the output pixel will be white.

The second half of Fig.7 presents the simulation results of the QCA morphological dilation operation, which confirms the correctness of the design. As it is shown, all possible value combinations of 5 inputs are applied to the circuit. The "sel" input is set to logic "1" which means that the design is configured for dilation operation. The output is set to logic "0" only when all inputs (i1 to i5) stay at logic "0" otherwise is set to logic "1" indicating the OR gate behaviour that leads to a successful morphological dilation operation.

5. Conclusion

This paper presents one novel configurable QCA design for the implementation of dilation or erosion morphological operation for image processing in binary images. The new QCA implementation provides parallel processing, high circuit performance, very low dimension and very low power consumption compared to conventional VLSI technology. The successful simulations and tests, which were executed in QCADesigner tool, show that the proposed design is capable of implementing either the erosion or the dilation morphological operations, configured by the value of one of its inputs.

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