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Design and Implementation of Voltage-Mode MIN/MAX Circuits

M. Soleimani*

[1]* *Department of Electrical Engineering, Bijar Branch, Islamic Azad University, Jahad Square, Bijar 66515-356, Iran.*

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Abstract

In this paper, a general architecture for analog implementation of MIN/MAX and other rank order circuits is presented. Based on general architecture, proposed MIN/MAX circuits are implemented. The proposed circuits are composed of a differential amplifier with merged n-inputs and a MCSAL circuit to choose the desired input. The advantages of the proposed structure are simplicity, very high resolution, very low supply voltage requirements, very low output resistor, low power dissipation, low active area and simple expansion for multiple inputs by adding only three transistors for each extra input. The post-layout simulation results of proposed circuits are presented by HSPICE software in 0.35-µm CMOS process technology. The total power dissipation of proposed circuits is about 110-µW. Also, the total active area is about 550-µm2 for five-input proposed circuits, and would be negligibly increased for each extra input.

Keywords: Voltage-Mode, MIN/MAX Circuits, Rank, Median.

1. Introduction

Minimum/Maximum (MIN/MAX) circuits are fundamental blocks in fuzzy systems and many nonlinear systems. Most of analog implementations for MIN/MAX circuits are typically based on the connection of n identical input cells to a common low-impedance output node. Competition input signals set the voltage at the output branch and, depending on the implementation, the output voltage will perform the MIN, MAX, MEDIAN, or other Rank-Order function.

The circuit in Fig.1(a) [1] is a CMOS analog voltage-mode MAX circuit based on voltage followers (VF) with a common source output node C. In this circuit, output voltage is equal to the maximum input voltage. The winner transistor corresponding to the maximum input voltage determines the voltage of node C, and carries a current equal to the diode-connected transistor (M_{out}). The major drawback of this structure is emphasized when two or more inputs are equal to the maximum value. In this case, the current residue of the tail source (I_B) would be divided equally between maximum inputs; the difference among the currents of winner and diode-connected transistors leads to a difference between overdrive voltages and creates an error in output voltage. For n-input MAX circuit, maximum error occurs when all inputs are equal, so, all of the input branches carry the current I_B/n, creating the overdrive voltage $\Delta V_{Mout}/\sqrt{n}$ (ΔV_{Mout} is overdrive voltage of Mout transistor). Therefore, the error value in output voltage could be obtained from the Eq.(1).

$$\text{Error} = V_{out}\text{-}V_{in,w} \simeq \left(1\text{-}\frac{1}{\sqrt{n}}\right)\Delta V_{M_{out}} \quad (1)$$

Equation (1) shows that maximum error value is increased by adding the number of maximum inputs, which is the major problem of MAX circuit in Fig.1(a), as discussed earlier in [9]. The circuit in Fig.1(b) is a CMOS analog current-mode MAX circuit based on voltage follower network, which uses n input cells. Each cell of Fig.1(b) has a voltage follower transistor M_{1i} (i=1, 2, ... , n) and a common source transistor (M_{Ci}) for gain enhancement a negative feedback loop. Main drawback of this circuit is that it is not appropriate to operate with low supply voltages and requires a minimum supply of $V_{DD,min}=2V_{GS} + |V_{DS(sat)}|$ (where $V_{DS(sat)}$ is the drain-source saturation voltage). Many other CMOS approaches for implementation of MIN/MAX circuits have been reported in literature (see, e.g., [3]-[9]).

The circuits in [4], [5] and [7] have used large number of transistors to implement a cell of MIN/MAX circuits which leads to the larger in area consumption. Meanwhile, in [4]-[7] the mismatch between current sources of input buffers reduces the precision and introduces an error in output voltage, and power consumption will be increased with increment of inputs number. The [3], [5] are not appropriate to operate with low supply voltage, and in [6] input/output swing is independent of V_{DD} and is given by $V_{in,pp}=V_{TH} - |V_{DS(sat)|,}$ (where V_{TH} is the threshold voltage), also, output resistor is very high. In the circuit of [9], peak-to-peak input/output swing is decreased by the overdrive voltage of transistor. In [8] we observe simply layered circuits of two-input comparators, in which for implementation of multi-input circuit, occupied area and power consumption will be increased.

In this paper, new voltage-mode MIN/MAX circuits have been presented. These circuits consist of a merged differential amplifier stage and a merged common-source with active load (MCSAL) stage. The proposed circuits use only a tail current source for each stage; therefore, the mismatch between tail current sources would not affect the error in output voltage. The total power dissipation of the

* E-mail address: sm_soleimani@yahoo.com
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proposed circuits is very low, constant and independent of inputs number because only two ndependent tail current sources are used. These circuits work with very high-precision and very low error in output because high accurate current-mirrors are used, and these circuits could be implemented in very small area, considering few transistors for 2-input implementation and only three extra transistors for each extra input. The output resistance of proposed MIN/MAX circuits is very low about multi ten ohms. Also, operating with very low supply voltage is another benefit of this work.

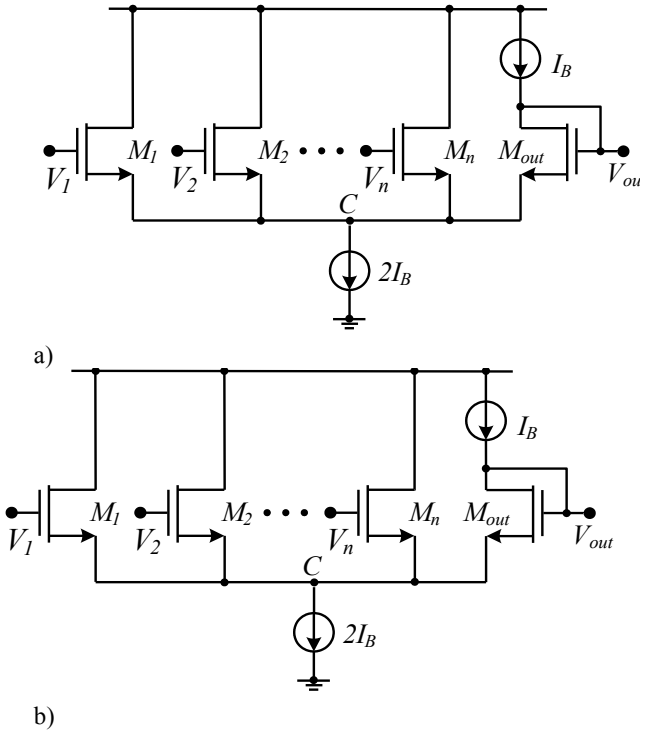

Fig. 1. (a) Conventional block of CMOS voltage-mode MAX circuit [1], (b) CMOS current-mode MAX circuit based on voltage followers [2].

In sect.2, The improved voltage-mode MIN/MAX circuits are described in details. The input/output swing, error measurement, power consumption, supply voltage requirements and output resistance are also analyzed. In sect.3, the post-layout simulation results which are performed by HSPICE software in 0.35-µm CMOS process technology, and also, the layout pattern of MIN/MAX circuits are presented. Finally section 4 concludes the paper.

2. The Proposed Voltage-Mode Min/Max

The improved MAX and MIN filters are illustrated in Fig.2. These circuits are composed of a merged n-input differential amplifier and an output stage used as MCSAL circuit. The MAX and MIN circuits generate highest and smallest value of inputs at output, respectively. Each branch of these circuits is composed of 3 transistors: M_I , M_C and M_P . The M_I is the input transistor which has a common node in its source (node C) with other input transistors and Mout and in fact, they have formed a voltage follower (VF) network. The M_C acts as a current mirror to produce a current equal to output current at winner branch, and M_P constitutes a MCSAL circuit with I_B current source (M_{B2}) to contain maximum or minimum of input

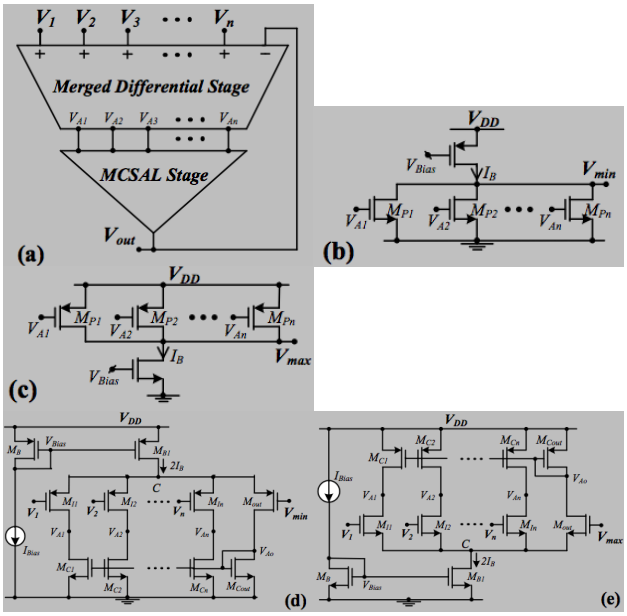

Fig. 2. (a) Architecture of proposed MAX circuit with MCSAL circuit in output, (b) MCSAL stage for implementation of MIN circuit, (c) MCSAL stage for implementation of MIN circuit, (d) Merged differential stage for implementation of MIN circuit, (e) Merged differential stage for implementation of MAX circuit.

For example, the proposed MIN circuit operates as follows. If we assume $V_1 < V_2 < ... < V_n$, then current of M_{out} and M_{I1} will be equal via current mirror consisting of M_{Cout} and M_{C1}. Also, output branch current at the merged differential amplifier will be compared with the current of input branches at nodes A_i (i=1, 2, ..., n) via current mirrors consisting of M_{Cout} and M_{Ci} transistors, and voltage of A_1 node will be determined via M_{P1} which is approximately equal to V_{GSMP1} , and voltage of nodes A_j (j=2, 3, ..., n) are almost equal to GND. Therefore, the transistors relevant to winner branch (first path), M_{I1}, M_{C1} and M_{P1} will operate in saturation region and the devices of others branches, M_{Ij} , M_{Cj} and M_{Pj} (j=2, 3, ..., n) will be in cutoff, triode and cutoff region, respectively. In this condition, only M_{P1} transistor from MCSAL stage will be on and the current I_B passes through M_{P1}, therefore, there will be a unity gain buffer as shown in Fig.3(a) and finally $V_{out} = V_1$. If we concentrate on Fig.3(a), then we can observe that the currents of differential amplifier branches will be equal to I_B. Therefore, the gate-source voltages of M_{P1} and M_{Cout} (which their sizes are the same) will be equal and voltage of A_1 and Ao nodes will be calculated from the Eqs.(2) and (3).

$$V_{A1} = \left|V_{GSM_{P_1}}\right| \quad (\tag{2}$$

$$V_{A0} = \left|V_{GSM_{Cout}}\right| \tag{3}$$

Which V_{GS} is the gate-source voltage of transistor. Because currents of M_{Cout} and M_{P1} are equal together, then, the gate- source voltages of M_{Cout} and M_{P1} will be equal, and according to above equations, $V_{Ao} = V_{A1}$. Therefore, drain-source voltages of M_{Cout} and M_{C1}, and also, M_{out} and M_{I1} will be equal, and because of this reason the currents of differential pairs will be exactly equal.

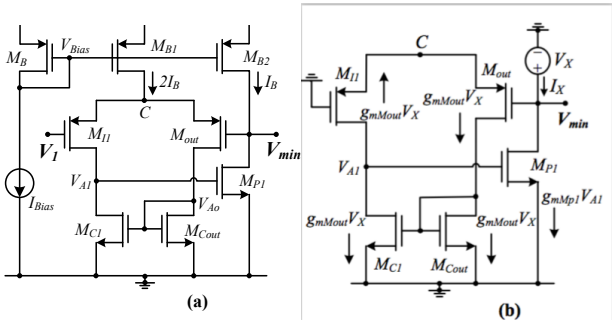

Fig. 3. (a) MIN circuit in case that only first branch is winner. (b) Small-signal equivalent circuit of Fig.3(a).

Then, according to Eq.(4), that is the current relation for MOS transistors in saturation region, and also, because the drain-source and gate-source voltages of M_{C1} and M_{Cout} transistors are the same and equal together, therefore, there will be high accurate current mirrors in this circuit, and then, the gate-source voltages of M_{out} and M_{I1} transistors (which their sizes are same) will be equal, too.

$$I_B = \frac{1}{2}\beta\left(V_{GS} - V_{TH}\right)^2\left(1+\lambda V_{DS}\right) \quad , \beta = \mu C_{ox}\frac{W}{L} \tag{4}$$

Then, by applying KVL in differential transistors of Fig.3(a), minimum output voltage will be calculated from the Eq.(5).

$$V_1 - V_{GSM_{I1}} + V_{GSM_{out}} - V_{out} = 0 \quad \Rightarrow \quad V_1 = V_{out} \tag{5}$$

In the other case, when m-inputs are in minimum state, the corresponding transistors with winner branches operate in saturation region and a current equal to $2I_B/(m + 1)$ will pass through M_{out} and M_{Ii}. The current of M_{Pi} transistors corresponding to winner branches will be equal to I_B/m and since current of output stage is not equal with current of differential pairs, the drain-source voltages of M_{Pi} and M_{Ci} will be different to some extent. Therefore, if assumed two-inputs or more to be in minimum state and transconductance of differential transistors to be β=2.16 mA/V^2 (at the worst case), the difference of drain-source voltages of M_{Ci} and M_{Cout} is about 25mV and according to Eq.(4), the maximum created error between current mirrors consisted of M_{Ci} and M_{Cout} transistors can be calculated from the Eq.(6).

$$\Delta I_B = I_{Cout} - I_{Ci} = \frac{\lambda\cdot\beta}{2}\left(V_{GS} - V_{TH}\right)^2\left(V_{DSM_{Cout}} - V_{DSM_{Ci}}\right)$$
$$= \frac{\lambda\cdot\beta}{2}\left(V_{GS} - V_{TH}\right)^2\left(25mV\right) \approx \lambda\cdot I_B\cdot 25mV \tag{6}$$

Which I_B is desired value of current. According to Eq.(6), created error (worst case) between current mirrors consisted of M_{Ci} and M_{Cout} transistors are very negligible and can be ignored. Then, the currents of differential amplifier branches consisted of M_{out} and M_{Ii} are equal, again, and the gate-source voltages of these transistors will be equal, too. Finally, according to Eq.(5), output voltage will be equal to minimum input voltages. Since the drain-source voltages of M_{Cout} and M_{Ci}, and also, M_{out} and M_{Ii} are equal, therefore, concerning on the precision of used current mirrors, we can consider a smaller value for the transistors length (L), and also, for transistors width (W), that leads to the reduction occupied area and achieving a better frequency response.

To calculate the maximum error in MIN circuit, we consider when m-inputs all are in minimum state. The transconductance of MOS transistor in saturation region can be described by Eq.(7).

$$g_m = \frac{2I_B}{(V_{GS}-V_{TH})} \tag{7}$$

As discussed earlier, since the current of merged differential amplifier branches is exactly equal, thus, the gate-source voltages of M_{out} and M_{I1} will be equal, too. Then, the transconductance of M_{out} and M_{I1} transistors will be equal. Therefore, the Eq.(8) which is obtained by combination of Eqs. (6) and (7) describes the maximum error value in output of MIN circuit.

$$\text{error} = V_{GSM_{out}} - V_{GSM_{Ii}} = \frac{\lambda.I_B}{g_{mM_{out}}}\left(V_{DSM_{Cout}} - V_{DSM_{Ci}}\right)$$
$$= \frac{\lambda.I_B.25mV}{g_{mM_{out}}} = \lambda.\Delta V_{M_{out}}.25mV \tag{8}$$

Therefore, according to above equation, the maximum error value in output is very negligible (Fig.5 confirms this speech), and we can say, that error is determined only by threshold voltage variations (Eq.(9)), and mismatching between transistors of differential pair, which is caused by fabrication process.

$$\Delta V_{TH} = \frac{A_{V_{TH}}}{\sqrt{WL}} = \frac{0.1t_{ox}}{\sqrt{WL}} \tag{9}$$

Which A_{VTH} and t_{ox} are the proportional coefficient and gate thickness of transistor, respectively.For calculate the output resistance of MIN circuit, we consider the circuit of Fig. 3(a), again. The small-signal equivalent circuit of Fig. 3(a) is shown in Fig. 3(b) by eliminating the current sources ($2I_B$=I_B=0). According to circuit of Fig. 3(b), voltage of node A_1 can be calculated from the Eq.(10):

$$V_{A1} = 2g_{mM_{out}}\cdot g_{mM_p}\left(r_{oM_{C1}} \parallel 2r_{oM_{I1}}\right) \tag{10}$$

The passing current through M_{P1} is the same with current of V_X, therefore:

$$I_X = g_{mM_{P1}}.V_{A1} \tag{11}$$

By substitution of Eq.(10) in Eq.(11), output resistor will be calculated as:

$$R_{out} = \frac{V_X}{I_X} = \frac{1}{2g_{mM_{out}}\cdot g_{mM_p}\left(r_{oM_{C1}} \parallel 2r_{oM_{I1}}\right)} \tag{12}$$

We can see that the output resistance of this circuit is much smaller than its counterpart in circuits of Fig.1(a) and Fig.1(b), and also, the circuits of [3]-[9], and this is another advantage of presented structure. The equivalent resistor of A_1 node is high, therefore, constructed pole in A_1 node is first pole of proposed circuits, and constructed poles in other nodes will happen in higher frequencies and will not any affect on the operation of these circuits.

Taking into consideration that the worst condition in swing calculation of MIN circuit is when only one of the inputs has the minimum value because of highest amount of current (I_B) passing through the winner branch and output branch. Therefore, if we assume first branch of proposed MIN circuit is the winner, the MIN circuit will be same as

Fig.3(a), and if all transistors in this circuit operate in saturation region, the voltage of node A_1 can be calculated as:

$$V_{A1} = V_{TM_{P1}} + \sqrt{\frac{2I_B}{\beta_{P1}\left(1+\lambda V_{DSM_{P1}}\right)}} \quad (13)$$

Which V_{TMP1} and β_{P1} are threshold voltage and transconductance coefficient of M_{P1}, respectively. The up and down input/output swing headroom of proposed MIN circuit can be calculated from the Eq.(14):

$$Swing = \begin{cases} Swing_{down} = Max\left(V_{o,\min}, V_{i,\min}\right) \\ Swing_{up} = Min\left(V_{o,\max}, V_{i,\max}\right) = V_{i,\max} \end{cases} \quad (14)$$

Which $V_{i,min}$ and $V_{i,max}$ are minimum and maximum swing values of input voltage, and $V_{o,min}$ and $V_{o,max}$ are minimum and maximum swing values of output voltage, respectively. To calculate the swing, we should obtain $V_{o,min}$ from the Fig.3(a). The value of $V_{o,min}$ will be calculated by assuming M_{P1} in saturation region. The condition in which M_{P1} remains in saturation region is: $V_{DSMP1} = V_{out} \leq V_{A1} + V_{TMP1}$. Then, Eq.(15) will be obtained:

$$V_{o.\min} = \sqrt{\frac{2I_B}{\beta_{P1}\left(1+\lambda V_{DSM_{P1}}\right)}} \quad (15)$$

Now, we want to calculate the value of input swing voltage. To calculate $V_{i,max}$, M_{B1} must remain in saturation region, so there must be $|V_{DSMB1}| \leq V_{DD} - V_{Bias} - |V_{TMB1}|$. Then, maximum of input swing voltage can be calculated from the Eq.(16):

$$V_{i.\max} = V_{DD} - \left|V_{TM_{I1}}\right| - \sqrt{\frac{2I_B}{\beta_{I1}\left(1+\lambda V_{DSM_{I1}}\right)}} - \sqrt{\frac{4I_B}{\beta_{B1}\left(1+\lambda V_{DSM_{B1}}\right)}} \quad (16)$$

Similarly, to calculate $V_{i,min}$, M_{I1} must remain in saturation region, then, there must be $V_{DGMI1} \geq V_{TMI1}$. Then, from the Eq.(17), it will be concluded that:

$$V_{i,\max} = V_{A1} - \left|V_{TM_{I1}}\right| = \left|V_{TM_{P1}}\right| + \sqrt{\frac{2I_B}{\beta_{P1}\left(1+\lambda V_{DSM_{P1}}\right)}} - \left|V_{TM_{I1}}\right| \quad (17)$$

In MIN circuit, bulk of differential transistors (M_{Ii}) is connected to the V_{DD}, so along with the decrement of input voltage value, threshold voltage of these transistors according to Eq.(18), will be increased, therefore, according to Eq.(17), $V_{i,min}$ will be decreased.

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right) \quad (18)$$

Which V_{SB} is source-bulk voltage of transistor. Finally, according to Eq.(14), the MIN circuit input/output swing will be determined by Vi,max and Vo,min and is given by $Swing_{pp} = V_{i,max} - V_{o,min}$.

The improved MIN/MAX circuits can operate with very low supply voltage. The minimum value of supply voltage for correct operation these circuits is $V_{DD,min} = |V_{GS}| + 2V_{DS(sat)}$, and also, peak-to-peak input-output swing is dependent to supply requirements and is given by $V_{in.PP} = V_{DD} - (|V_{GS}| + 2V_{DS(sat)})$. This feature enables us to use these circuits in other CMOS submicron technologies such as 0.25-µm and 0.18-µm with 0.4V threshold voltages for both NMOS and PMOS transistors.

The total power dissipation is consisted of three separate terms; the first is allocated to power consumption of merged differential amplifier block, the second term is the power consumed in MCSAL block and the third term is the power used to generate main bias current. The total power dissipation can be calculated from the Eq.(19).

$$P_{out} = 2I_B \cdot V_{DD} + I_B \cdot V_{DD} + I_{Bias} \cdot V_{DD} = \left(3I_B + I_{Bias}\right) \cdot V_{DD} \quad (9)$$

Which I_{Bias} is main bias current of proposed circuits. According to Eq.(19), the power dissipation is constant and independent of inputs and doesn't change with the increment of inputs number.

As discussed earlier, the proposed MAX circuit is attained if the complementary MOS version of MIN circuit is adapted, which is shown in Fig.3. The MAX circuit operates as similar as the MIN circuit, as explained earlier. All relations of this circuit would be realized in the same way as discussed for proposed MIN circuit. The proposed architecture can be a rank-order circuit by replacing the MCSAL circuit in MIN circuit with CMOS inverting amplifier. The Rank-Order circuit is determined by the total aspect ratio of the CMOS inverting amplifier transistors. The main limitation of this circuit is high power consumption and the dependency of its resolution to the number of inputs (n).

3. Simulation Results and Layout Pattern

The proposed MIN/MAX circuits of Fig.2 and Fig.3 were implemented in 0.35-µm CMOS technology and with the following transistor dimensions (in units of λ): $(W/L)M_{B1}=2(W/L)M_{B2}=10/1$, and (W/L)=5/0.5 for other NMOS and PMOS transistors, respectively. The threshold voltages for NMOS and PMOS transistors in our process are 0.55V and -0.75V, respectively. Simulations results were performed with I_B=10µA, V_{DD}=3.3V, load capacitor C_L=5pF, and also, mismatching between differential transistors is considered 1% and threshold voltage deviation (ΔV_{th}) is considered ±3mV (Eq. 9). The HSPICE Monte Carlo analysis for post-layout transient simulations of MIN/MAX circuits with five inputs (n=5) is shown in the Fig.4. While, a triangular wave V_{in1} was applied to two inputs, a sinusoid wave V_{in2} was applied to two other inputs, and a fixed voltage V_{in3} was applied to one other input of proposed circuits.

The Fig.5 shows static behavior and output error of proposed MAX and MIN circuits by Monte Carlo analysis. In this case, a varying voltage V_{in1} was applied to one input, while a fixed voltage V_{in2}=1.5V was applied to other four inputs. As shown, V_{out} follows very closely, even in the corner regions, where the error is not any larger than elsewhere. The estimated voltage swing for proposed MAX and MIN circuits have obtained between $0.83V \leq V_{in} \leq 3.12V$ and $0.1V \leq V_{in} \leq 2.12V$, respectively. Also, the created error in output for proposed circuits in maximum allowable input/output swing have obtained between -3mV/+3mV and -2mV/+4mV, respectively. Also, simulations were

performed in process corners and in this case, simulated results were almost the same results that are shown in Figs.4 and 5.

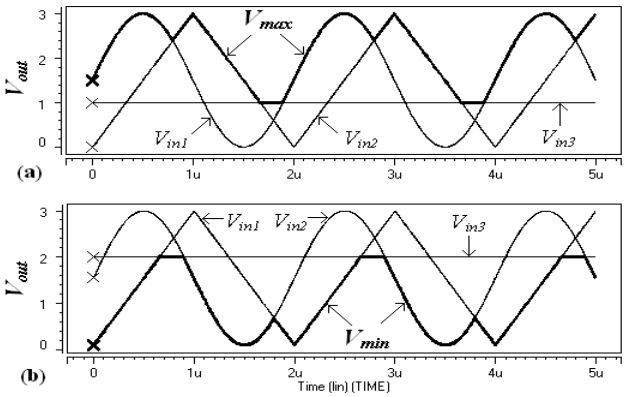

Fig. 4. The Monte Carlo Analysis of proposed circuits transient response. (a) MAX circuit. (b) MIN circuit.

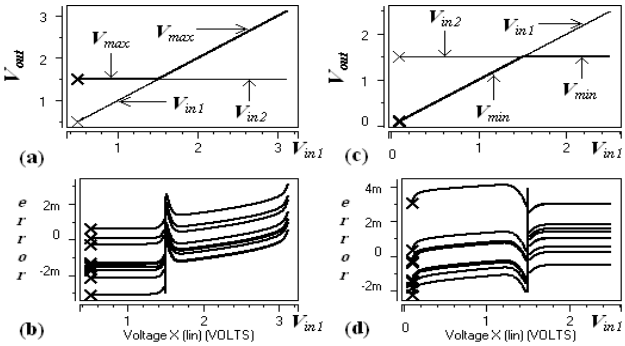

Fig. 5. The Monte Carlo Analysis of proposed circuits static behavior. (a) Static behavior of MAX circuit. (b) Static output error in MAX circuit. (c) Static behavior of MIN circuit. (d) Static output error in MIN circuit.

The Fig.6 shows accuracy of proposed circuits when difference between input voltages are close together. In this case, a varying voltage V_{in1} was applied to one input, while a fixed voltage V_{in2}=1.5V was applied to two other input, and a fixed voltage V_{in3}=1.51V was applied to two other input. Layout pattern of the proposed MAX and MIN circuits are illustrate in Fig.7. The active area for proposed circuits were about 26µm×21µm for five-input circuits (n=5).

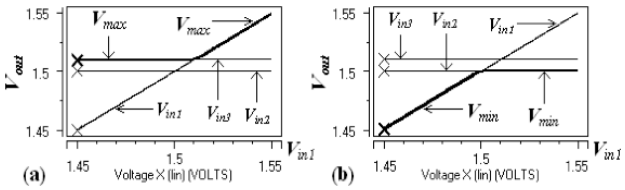

Fig. 6. HSPICE simulation results to shows accuracy of proposed circuits with input voltages close together. (a) MAX circuit. (b) MIN circuit.

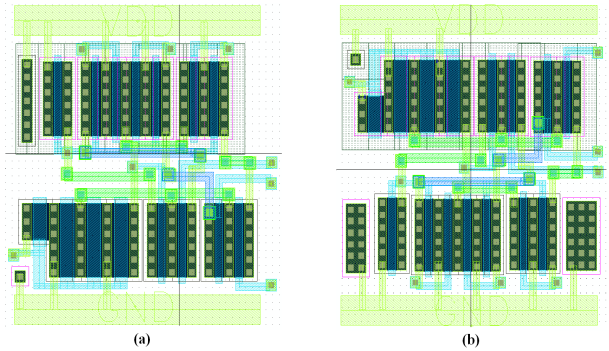

Fig. 7. Layout pattern of the proposed circuits for five-input circuits (n=5). (a) MAX circuit. (b) MIN circuit.

4. Conclusions

In this paper, a general architecture for analog implementation of MIN/MAX and other rank-order circuits is presented. This architecture contains a differential amplifier with merged n-inputs and a MCSAL circuit to choose the desired input in MIN/MAX circuits. The architecture can be a rank-order circuit by replacing the MCSAL circuit with CMOS inverting amplifier. The advantages of the proposed structure are simplicity, high operating frequency, very high resolution, very low supply voltage requirements, very low output resistor, low power dissipation, low active area and simple expansion for multiple inputs by adding only 3 transistors for each extra input. Table 1, compares the proposed and previous works, and shows the better results in comparison with other works.

Table 1. The comparison of this work and other similar works.

	[3]	[4]	[5]	[7]	[9]	**PROPOSED**
Technology	2-µm	1.6-µm	0.8-µm	0.5-µm	0.35-µm	**0.35-µm**
Power Supply	5-V	5-V	5-V	3-V	3.3-V	**3.3-V**
Error (mV)	±10-mV	±15-mV	---	---	±12-mV	**±4-mV**
Number of Trans.	3n+5	7n+3	6n+3	5n+3	3n+4	**3n+3**
Output Resistor	Low	Very Low	Very Low	Low	Low	**Very Low**
Occupied Area	650µm×100µm 2-inputs	56µm×358µm 9-inputs	---	190µm×86µm 3-inputs	29µm×30µm 5-inputs	**26µm×21µm 5-inputs**
Power Dissipation for 2-inputs	800-µW I_B=10µA	250-µW I_B =10µA	200-µW I_B =10 µA	200-µW I_B =10µA	85-µW I_B =10µA	**110-µW I_B =10µA**

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