Low complexity Breadth First Search Sphere Detector for MIMO Systems

Shirly Edward.A[1,*] and Malarvizhi.S[2]

[1]*Department of ECE,SRM University,Vadapalani,Chennai ,Tamil Nadu,India*
[2]*Department of ECE,SRM University,Kattankulathur,Chennai ,Tamil Nadu,India*

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Abstract

Multiple Input Multiple Output (MIMO) technology is the key to meet the demands for data rate and link reliability of modern wireless communication system, such as 3GPP-LTE.The full potential of such a system can be achieved only by high performance detection algorithms, which exhibit prohibitive computational complexity. Therefore, in this paper, a low complexity and highly parallel Breadth First search Sphere Detector (BFSD) is proposed for MIMO detection, which takes forward only the symbol set with minimum partial Euclidean distances (PEDs) of the expanded node in the tree search process. We had designed a BFSD scheme for 16QAM modulation with 2 x 2 and 4 x4 antenna configurations and implemented on a state-of-the-art Xilinx Virtex 5 FPGA device. The results indicate that with less computational complexity compared with the literature the detector can achieve a throughput of up to 98Mbps which makes it suitable for 3GPP-LTE uplink transmission.

Keywords: MIMO, Sphere detector, Breadth first search, Latency, VLSI, Throughput.
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1. Introduction

Current day applications of wireless communication systems are based on the continuous increase in the data rate, system capacity and quality of service. It is well known that MIMO systems can achieve an extra ordinary spectral efficiency near Shannon bound and also increase the capacity. Communication reliability improves with the use of multiple antennas at both sides of the wireless link [1]. Fourth generation (4G) mobile communication systems incorporate MIMO technology to enhance voice and data transmission, and several wireless communication standards such as IEEE 802.11n wireless LAN,IEEE 802.16e WiMax and 3GPP-LTE already include MIMO techniques. The potentials of MIMO technology can be exploited at the cost of high computational complexity and high computing power at the transmitter and receiver end. Therefore, the key problem in the deployment of MIMO wireless system design is to reduce the hardware complexity of receivers.

For uncoded MIMO systems, Maximum Likelihood detector would be the optimal receiver, but the exponential computational complexity involved makes this approach unattractive. An alternative approach called sphere decoding algorithm was proposed, which reduces the computational complexity by considering symbols that lie only inside the hypersphere. In literature, different types of algorithms and VLSI implementations of sphere decoder are found. In [2], Garrett et.al has done a complexity analysis and shown that it is feasible to achieve near ML performance for 4x4 16QAM using spherical techniques, the VLSI implementation of which is reported in [3]. However the conventional sphere decoder implementations suffer from non-uniform throughput, which is a main drawback for communication systems, which expect a constant performance. Guo and Nilsson [4] proposed the K-best sphere decoder algorithm which provides constant throughput and supports the hard and soft outputs.

In this paper, we propose a novel approach for Breadth First search Sphere Decoding algorithm aimed to reduce area and power consumption while maintaining constant throughput. The shortcomings in the previous approaches and the techniques used to handle them are presented. In Section 2, a brief review of a MIMO system model and the tree search process are presented. In Section 3, the proposed Breadth First Search Sphere Decoder (BFSD) algorithm and the architecture blocks are explained. The VLSI implementation of the proposed method and its complexity analysis are presented in Section 4. Section 5 concludes the paper.

2. MIMO Detection Algorithm

In this section, the MIMO system model and the sphere decoding algorithm are reviewed briefly addressing in particular the breadth- first search strategy. The modified algorithm is presented in Section 3.

2.1 System Model
Let us consider a MIMO communication system that employs M transmit antennas and N receive antennas. Assuming a Rayleigh fading channel, the system can be modeled as

$$y = Hs + n \tag{1}$$

Where s is the M x 1 transmitted symbol vector, H is the N x M channel matrix, n is the N x 1 independent identically distributed white Gaussian noise vector and y is the N x 1 received symbol vector. In our paper, we assume without loss of generality that the number of transmitter antennas and the number of receiver antennas are equal.ML detection minimizes the difference between the received signal vector and the transmitted symbol vector distorted by the channel. The ML estimation for a transmitted symbol vector s is stated as

$$\tilde{s} = \arg\min ||y - Hs||^2 \qquad (2)$$

$$s \in O^M$$

Where O^M is the set of possible values for the transmitted symbol. A direct implementation of ML detection leads to an exhaustive search which is practically unfeasible. Therefore, Sphere decoding algorithm has been introduced to reduce the complexity.

2.2 Sphere Decoding Algorithm
Partial Euclidean Distance (PED) Calculation and the tree traversal process are the two main parts of Sphere Decoding algorithm.SD makes use of an efficient pruning criterion and takes into account only the lattice points that are inside a hypersphere of a given radius r. The Sphere constraint is expressed by the following inequality.

$$||y - Hs||^2 < r^2 \qquad (3)$$

The Equation (1) can be decomposed as follows:

$$||\hat{y} - Rs||^2 = \sum_{i=1}^{M} ||\hat{y}_i - \sum_{j=i}^{M} r_{ij} s_j||^2 \qquad (4)$$

Where $\hat{y} = Q^H y = Rs^{ZF}$, Q and R are got from the QR decomposition of H and r_{ij} is the element of upper triangular matrix R. The PED equation can be rewritten as

$$d_i = d_{i+1} + |e_i|^2 \qquad (5)$$

$$|e_i|^2 = |\hat{y}_i - \sum_{j=i}^{M} R_{ij} s_j|^2 = |b_{i+1} - R_{ii} s_i|^2 \qquad (6)$$

Where

$$b_{i+1} = \hat{y}_i - \sum_{j=i+1}^{M} R_{ij} s_j \qquad (7)$$

Starting from the last element i=M the detection process recursively finds the shortest path with the minimum PEDs. The tree traverse can be reduced because the current PED includes the PED from the previous search. If the calculated PED is larger than the search radius r the corresponding traverses are terminated because the PEDs must be outside the hypersphere. Therefore, the initial radius is set to infinity to alleviate the problem of initial radius choice[3].
The tree traversal can be depth first or breadth first based on their search strategy. The depth first search algorithms

process only one candidate symbol vector at a time, whereas the breadth first search algorithms process all the partial candidate symbol vectors on each level before moving to the next level. The K-best breadth first search algorithm [5] keeps the K best nodes which have the smallest accumulated PEDs at each level. After completing the tree search process, we will have K leaves with the smallest PEDs. Each path in the tree corresponds to a symbol vector s. The path with the smallest PED is the detected symbol vector. The K-best algorithm can guarantee a constant throughput and has BER performance that is close to ML detector [6].

2.3. Real Value Decomposition
In practice, the M-dimensional complex signal model in Equation(1) is decomposed into 2M dimensional real valued signal model according to the Eq.(8)

$$\begin{bmatrix} R\{y\} \\ I\{y\} \end{bmatrix} = \begin{bmatrix} R\{H\} & -I\{H\} \\ I\{H\} & R\{H\} \end{bmatrix} \begin{bmatrix} R\{s\} \\ I\{s\} \end{bmatrix} + \begin{bmatrix} R\{n\} \\ I\{n\} \end{bmatrix} \qquad (8)$$

This equation results in a tree that is twice as deep as the original tree and it contains smaller number of children per node, but the number of leaves remains unchanged.

3. Breadth First Search Sphere Detector (BFSD) Technique

In [7], Winner path extension technique is discussed in which all the children of a node are not extended in parallel. The minimum metric child among all these nodes is selected as the winner and it is taken as the first among K-best extended paths. The winner node is extended to its next best child and the process is repeated. This technique solves the problem of sorting but parallel path extension only can achieve high throughput at the cost of both area and power[5]. Therefore, we propose a novel parallel processing approach called Breadth First Search Sphere Detector (BFSD) which is shown in Figure1. It is a modified version of winner path technique and it chooses the symbol set with minimum PED in a particular node and extends to the next level. The idea is to find the symbol set with minimum path metric in each layer for various nodes depending upon the constellation size and in the last layer find the complete symbol set with the minimum partial Euclidean distance. The algorithm for the technique is given by:
At each layer i, for each branch of K we do the following:

- Expand each node with their leaf nodes. Compute the PEDs for each symbol set.
- Sort the PEDs to find the minimum and store along with the symbol set and evict the remaining symbol set from the tree search process.

Repeat the steps for all K branches and at the final layer the symbol set with minimum PED will give the hard output detection solution. The parameter K refers to the number of symbols in the constellation.
The proposed BFSD unit shown in Figure 2 for one layer of the tree consists of a Block RAM (BRAM) unit, the Metric Computation unit and the sorter unit. The BFSD unit is designed in such a way that one layer of the tree is always processed in one pipeline stage. The Block RAMs are constructed using look up tables once per channel realization

and reused to calculate the PED for each new symbol set. The Metric Computation Unit (MCU) computes the PEDs of all children of a parent node and sends it to the sorter unit where the minimum PED is found and stored in data store memory. The BFS-best unit determines the minimum PED for each symbol set and stores in memory and delivers them to the next pipeline stage. Therefore, altogether 2M identical copies of the BFS unit form the 2M pipeline stages of the detector.
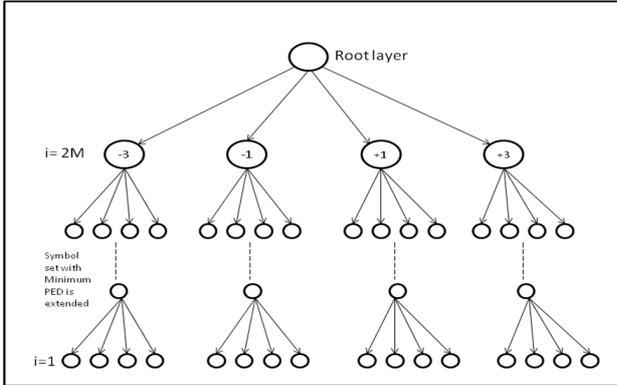

Fig. 1 Conceptual flow of the proposed Breadth first search Sphere Detector(BFSD) Technique
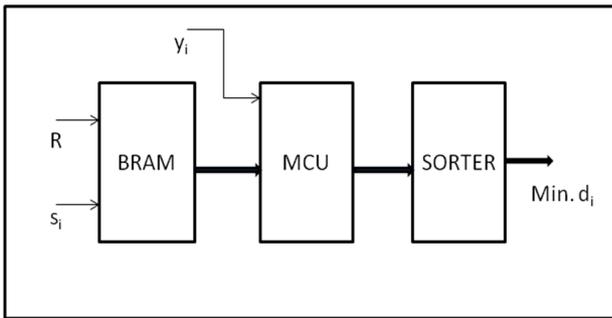

Fig. 2 Breadth First Search Sphere Detector (BFSD) unit

In each layer, for each branch the children node are processed together in parallel, as there is no data dependency between them. In the root layer, all the branches are processed in one cycle, while in lower layers, four clock cycles are needed to process all the 16 nodes. The high level architecture for MCU made use of in the BFSD unit is shown in Figure 3.The partial Euclidean distances are calculated for every node in the MCU.
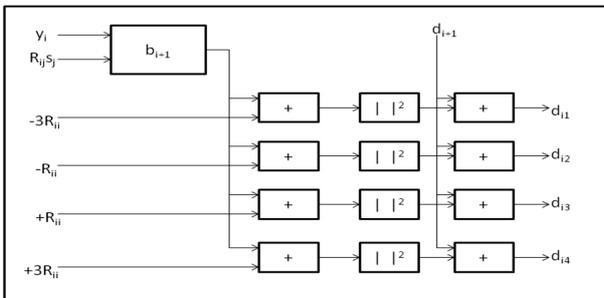

Fig. 3 Metric Computation Unit

It is based on Batcher's parallel bitonic sorting algorithm[8]. Bitonic sorting algorithm was considered the most practical parallel sorting algorithm for many years.

Figure 4 shows a merge and sort unit which is used for finding the minimum PED. The MSU consists of 3 comparators and multiplexers, where only 2 comparators are serially connected in critical path.
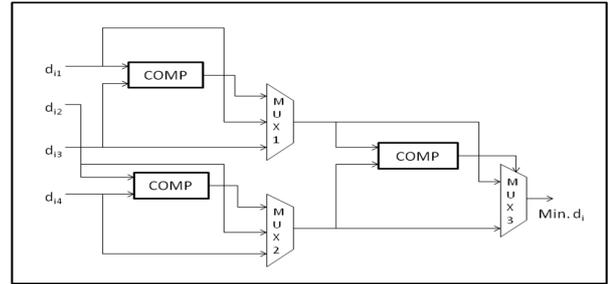

Fig. 4 Merge and Sort unit (MSU)

4. VLSI Implementation

The proposed BFSD unit was implemented using the blocksets in Xilinx System Generator. It is a MATLAB-Simulink based design tool for Xilinx's line of FPGAs. The Xilinx blockset consists of high-level blocks that map the intellectual property (IP) cores that have been handcrafted for efficient implementation in the target Xilinx FPGA.

We had considered a 16 QAM modulation with 2 x 2 and 4 x 4 MIMO antenna configurations. We consider only a slowly varying Rayleigh fading channel. The complex channel matrix leads to higher hardware complexity as shown in [9] and [10]. Therefore, the complex channel matrix H is converted into real channel matrix by Real Value Decomposition (RVD).The real valued matrix is fed to the preprocessing unit where QR decomposition was performed. The upper triangular matrix R is fed as input to the Block RAM together with the symbol combination. The Xilinx System Generator FPGA implementation of the BFSD unit on a Xilinx Virtex-5 FPGA, xc5vsx95t-3ff1136 for 16-bits precision are presented in Table 1. The results clearly show that the hardware complexity is greatly reduced by our proposed work compared to [11] and [12].

Table 1 . FPGA Resource utilization comparison of the BFSD unit

Reference	Proposed work		[11]	[12]
Device	Xilinx Virtex-5 FPGA			
Antennas	2x2	4x4	4x4	4x4
Modulation	16QAM	16QAM	16QAM	16QAM
Number of Slice registers(58,880)	582	1718	27,115	3459
Number of Slice LUTs(58,880)	6208	16872	33,427	-
Number of BRAMs	20	72	Not reported	0
Number of DSP48Es(640)	84	212	321	36

The latencies of the BFSD unit are presented in Table 2 for 2 x 2 MIMO system, 16 QAM modulation. From the table it is clear that for the topmost layer, all the PEDs are calculated in parallel and the latency is 4 clock cycles. The remaining layers also require 4 clock cycles for calculating the PEDs and 2 clock cycles for sorting. Thus the unit takes 22 clock cycles to find the hard detected output through the entire tree traversal. Similarly the latencies of BFSD unit are presented in Table 3 for 4 x 4 MIMO system, 16 QAM

modulation. The overall latency was found to be 46 clock cycles.

Table 2. Latencies of the BFSD unit for 2 x2, 16 QAM modulation

Blocks	Latency in clock cycles
Layer 4	4
Layer 3 to layer 1+ Merge and Sort	18
Total	22

The power analysis results are estimated by Xilinx Xpower Analyzer using System Generator. The results are shown in Table 4.

Table 3. Latencies of the BFSD unit for 4 x 4, 16 QAM modulation

Blocks	Latency in clock cycles
Layer 8	4
Layer 7 to layer 1+ Merge and Sort unit	42
Total	46

Table 4. Power Analysis Results

Resources	2x2, 16 QAM	4x4, 16 QAM
Clocks	76mW	112mW
Logic	59mW	172mW
Signals	139mW	346mW
BRAMs	101mW	365mW
DSPs	31mW	77mW

The maximum throughput of the BFSD unit is calculated by the Equation 9

$$Throughput = f_{max} \frac{\log_2(M_c)N}{C} \tag{9}$$

Where f_{max} is the maximum clock frequency, M_c is the constellation size, N is the antenna number and C is the number of clock cycles required to calculate the PEDs through the entire tree traversal. For our BFSD unit with 2 x 2 MIMO system, C= 22 and with 4 x 4 MIMO system, C=46. Table 5 presents the throughput analysis and the maximum throughput for the detection scheme would be 98Mbps.

Table 5. Throughput Analysis

Parameter	2 x 2, 16 QAM	4 x 4, 16 QAM
Throughput	98Mbps	91Mbps
Maximum Frequency	270.976MHz	264.367MHz

5. Conclusion

A modified Breadth First search Sphere Decoder has been proposed for MIMO detection, which helps in reducing the computational complexity by optimizing the tree search process. Compared with the previously published pipeline architectures, the proposed parallel processing reduces the cost of hardware resources and maintains constant throughput. This makes it suitable for practical applications with balanced performance and hardware complexity and can also be extended to meet the increasing demand of future wireless communication standards.

References

1. Gesbert.D,Shafi.M,Shiu.D.S,Smith.P,Naguib.A,"From theory to practice: an overview of MIMO space-time coded wireless systems, "IEEE Journal of Selected areas in communication, Vol.21,pp.281-302,2003.
2. David Garrett et.al," Silicon complexity for Maximum Likelihood MIMO Detection using spherical techniques," IEEE Journal of Solid State Circuits, Vol.39,pp.1544-1552,2004.
3. A.Burg,M.Borgmann,M.Wenk,M.Zellweger,W.Fichtner and H.Bolcskei, "VLSI Implementation of MIMO detection using the sphere decoding algorithm," IEEE Journal of Solid-State Circuits,Vol.40,pp.1566-1577,2005.
4. Guo and P.Nilsson," Algorithm and implementation of the K-best sphere decoding for MIMO detection," IEEE Journal of Selected areas in communication, Vol.24,No.3,pp.491-503,March 2006.
5. S.Chen et.al., "Relaxed K-best MIMO signal detector design and VLSI implementation," IEEE Transaction on Very Large Scale Integration(VLSI),Vol.15,pp.328-337,2007.
6. K Wong C.Tsui, R.-K.Cheng and W.Mow, "A VLSI Architecture of a K-best Lattice Decoding Algorithm for MIMO Channels," in Proc.IEEE International Symposium on Circuits and Systems,Vol.3,Finland,2002(Helsinki,Finland)273-276.
7. Mondal,Sudip,Eltawil,Ahmed.M,Salama,Khaled N,Shen,Chung-An, "Design and implementation of a Sort-Free K-best Sphere decoder," IEEE Transactions on Very Large Scale Integration(VLSI),Vol.18,pp.1497-1501,2010.
8. K.E. Batcher," Sorting networks and their applications," in Proceedings AFIPS Spring Joint Comput. Conference, Vol.32,1968, pp. 307-31.
9. L.G.Barbero,J.S. Thompson," Rapid prototyping of a fixedthroughput sphere decoder for MIMO systems," in Proceedings of the IEEE ICC, Vol.7,Turkey,2006, pp.3082-3087
10. M.S.Khairy, M.M.Abdallah,S.E.-D.Habib," Efficient FPGA implementation of MIMO detector for mobile WiMAX system," in Proceedings of the IEEE ICC,Germany,2009,pp.1-5.
11. Chris Dick et.al, "Design and architecture of spatial multiplexing MIMO decoders for FPGAs," in 42nd Asilomar Conference on Signals,Systems and Computers, 2008, pp.160-164.
12. Markus Myllala," Detection Algorithms and Architectures for wireless spatial multiplexing in MIMO-OFDM systems", Ph.D. Dissertation, University of Oulu, Finland, 2011.