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VDTA Based Electronically Tunable Purely Active Simulator Circuit for Realizing Floating Resistance

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Abstract

This paper proposes a new active synthetic floating resistor circuit employing three voltage differencing transconductance amplifiers (VDTAs). The proposed configuration enjoys following advantageous features; (a) purely active realization (b) electronically tunable resistance (c) no external component matching constraint(s) (d) good non-ideal behavior and (e) low sensitivity values. The workability of proposed resistor simulator has been verified by an application example of voltage mode low-pass filter. To validate the theoretical analysis SPICE simulations with TSMC 0.18µm CMOS process parameters have been performed.

Keywords: VDTA, Synthetic resistor, floating resistor, electronic control, purely active simulation circuit

1. Introduction

Active simulation of floating passive elements (resistors/capacitors/inductors) is a fascinating research area for analog circuit designers and researchers. Several floating passive component simulators have been proposed in [1]-[16] and reference cited therein. The floating resistor is an integral part of analog circuits but the use of resistor in floating state is not advisable from the viewpoint of monolithic integration as a floating resistor need more chip area than a grounded resistor and also it is very difficult to design such a resistor with exact resistance value. Moreover, the resistance is fixed and cannot be changed as per requirement. So, the active simulation of floating resistors has become a popular research area in which a floating resistor is realized either by using active element(s) alone or by using active element(s) along with grounded resistors(s.).There are several synthetic floating resistor configurations available in literature but electronic tunability is available with very few configurations [11-16]. The negative floating resistor proposed in [11] was purely active realization and need four current controlled second generation current conveyors (CCCII). The configuration proposed in [12] employs one second generation current conveyor (CCII) and one operational transconductance amplifier (OTA) along with two grounded resistors. A current backward transconductance amplifier (CBTA) based floating resistance simulator circuit employing two CBTA and three grounded resistors has been presented in [13]. An improved CBTA based floating resister simulation circuit has been proposed in [14] which employs single CBTA along with two grounded resistors but this circuit needs current/voltage gain matching constraints. Positive/negative floating resistance simulation circuits employing two/three current follower transconductance amplifiers (CFTA) have been proposed in [15] but in both the cases matching condition of transconductances are required. The configuration proposed in [16] employs two DVCC and three grounded resistors but in non ideal conditions it does not simulate lossless floating resistor.

Therefore, the aim of this paper is to propose new electronically tunable synthetic floating resistor configuration employing three VDTAs with no requirement of any external grounded resistor. The proposed circuit exhibits low sensitivity values and excellent non- ideal behavior.

2. Proposed Configuration

The voltage differencing transconductance amplifier (VDTA) is one of the active elements which have been introduced in [17]. It provides currents and voltages at different terminals with electronically tunable transconductance gains. Therefore, VDTA block is very suitable for synthesis and design of active circuits with electronic tunability feature. Fig.1 shows the symbolic representation of VDTA, where P and N are input ports, z is auxiliary port and X+ and X- are output ports with all ports at high impedance level. The CMOS implementation of VDTA [18] has been shown in Fig. 2.

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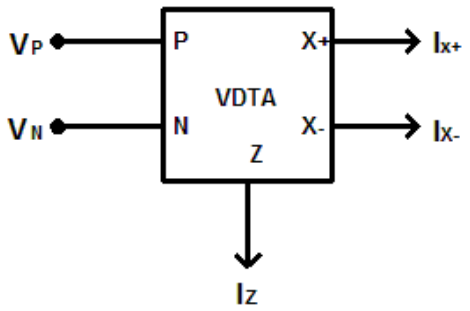


Fig. 1. VDTA symbolic representation

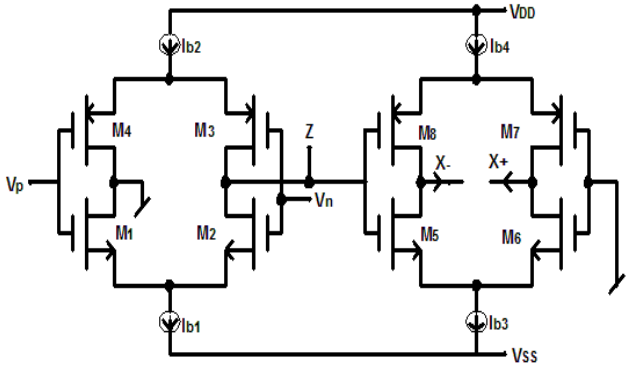


Fig. 2. CMOS implementation of VDTA [18]

The port relations of ideal VDTA shown in Fig. 1 can be characterized by following hybrid matrix ;

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m_1} & -g_{m_1} & 0 \\ 0 & 0 & g_{m_2} \\ 0 & 0 & -g_{m_2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \tag{1}$$

The trans-conductance gains g_{m1} and g_{m2} of CMOS VDTA shown in Fig. 2 are given as

$$g_{m_1} = \frac{g_3 + g_4}{2} \tag{2}$$

$$g_{m_2} = \frac{g_5 + g_8}{2} \text{ or } g_{m_2} = \frac{g_6 + g_7}{2} \tag{3}$$

Where, g_n is the transconductance of n^{th} MOS transistor given as

$$g_n = \sqrt{I_{B_n} \mu_n C_{OX} \left(\frac{W}{L}\right)_n} \tag{4}$$

where, μ_n is carrier mobility, C_{OX} is capacitance of gate-oxide layer per unit area, W is MOS transistors's effective channel width, L is effective channel length and I_{Bn} is bias current of n^{th} transistor.

VDTA find several applications in designing of analog filters [19-21], oscillators [22] and inductor simulators [23] but there is no application in simulation of floating resisters has been reported so far. So, this paper is an effort to fill this void

The proposed purely active floating resister simulator is shown in Fig. 3.

The Routine circuit analysis of configuration shown in Fig. 3 yields short circuit admittance matrix as

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_A} g_{m_B}}{g_{m_3}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \tag{5}$$

Which simulate a floating resistor with resistance value:

$$R_{eq} = \frac{g_{m_3}}{g_{m_A} g_{m_B}} \tag{6}$$

for $g_{m2} = g_{m6} = g_{mA}$ and $g_{m1} = g_{m5} = g_{mB}$

Where (g_{m1}, g_{m2}), (g_{m3}, g_{m4}) and (g_{m5}, g_{m6}) are the transconductances of VDTA-1, VDTA-2 and VDTA-3 respectively. These transconductance matching conditions can be meet easily just by equating the bias currents of VDTAs.

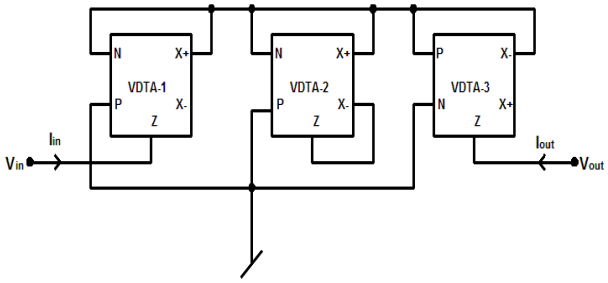


Fig. 3. Proposed purely active floating resistor simulator

One can observe from Eq. 6 that the resistance of proposed synthetic resistor can be controlled electronically by varying transconductances g_{m1}, g_{m2}, g_{m3}, g_{m5} or g_{m6}. It is important to note that the presented circuit can also simulate negative floating resistor (-R) by appropriate interchanging of p and n and/or x+ and x- ports of VDTAs. Such negative resistor simulator can be used for parasitic cancellation purpose.

3. Non-Ideal and Sensitivity Analysis

In the non ideal case, the VDTA can be characterized by the following equations;

$$I_Z = \beta_Z g_{m_1} \left(V_P - V_N\right) \tag{7}$$

$$I_{X+} = \beta_{x+} g_{m_2} V_Z \tag{8}$$

$$I_{X-} = -\beta_{x-} g_{m_2} V \tag{9}$$

where β_Z, β_{X+} and β_{X-} are non ideal transconductance gain errors.

To check the behaviour of presented configuration under non ideal conditions, it is revisited considering the non ideal model of VDTA described by Eq. 7-9. The short Circuit admittance matrixes and floating resistances values of proposed simulator under the influence of VDTAs non idealities can be re-expressed as

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_A} g_{m_B} \beta_{x_2-} \beta_A \beta_B}{g_{m_3} \beta_{x_2+} \beta_{z_2}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (10)$$

and

$$R_{eq} = \frac{g_{m_3} \beta_{x_2+} \beta_{z_2}}{g_{m_A} g_{m_B} \beta_{x_2-} \beta_A \beta_B} \quad (11)$$

For $g_{m2} = g_{m6} = g_{mA}$, $g_{m1} = g_{m5} = g_{mB}$, $\beta_{x1+} = \beta_{x3-} = \beta_A$ and $\beta_{Z1} = \beta_{Z3} = \beta_B$.
where (β_{Z1}, β_{X1+}, β_{X1-}), (β_{Z2}, β_{X2+}, β_{X2-}) and (β_{Z3}, β_{X3+}, β_{X3-}) are the transconductance gain errors of VDTA-1, VDTA-2 and VDTA-3 respectively.

It is clear from Eq. 11 that even under the non ideal conditions the proposed configuration simulates the lossless floating resistor without any lossy term.

The sensitivity figures of resistance of simulated floating resistor with respect to transconductance gains/ gain errors are found as;

$$S_{g_{m1}}^{R_{eq}} = S_{g_{m2}}^{R_{eq}} = S_{g_{m5}}^{R_{eq}} = S_{g_{m6}}^{R_{eq}} = -1, S_{g_{m3}}^{R_{eq}} = 1,$$

$$S_{\beta_{x2-}}^{R_{eq}} = S_{\beta_{x1+}}^{R_{eq}} = S_{\beta_{x3-}}^{R_{eq}} = S_{\beta_{z1}}^{R_{eq}} = S_{\beta_{z3}}^{R_{eq}} = -1, S_{g_{m4}}^{R_{eq}} = 0,$$

$$S_{\beta_{x2+}}^{R_{eq}} = S_{\beta_{z2}}^{R_{eq}} = 1 \quad (12)$$

So, all the sensitivity figures are low and not more than unity in magnitude.

4. Effects of Parasitics

At high frequency, the terminal parasitic of VDTA comes into the picture and effect the performance of a VDTA based circuit. A conventional VDTA along with its port parasitic has been shown in Fig. 4.

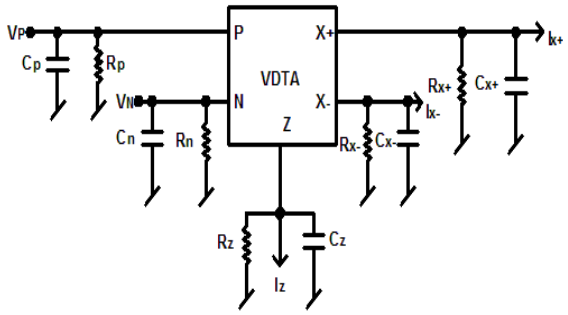


Fig. 4. Conventional VDTA with port parasitics

§To study the effects of terminal parasitic of VDTAs on proposed resistance simulator configuration, this configuration was examined including port parasitic of VDTA. Fig. 5 shows the proposed resistance simulator with port parasitic of VDTA-1, VDTA-2 and VDTA-3.

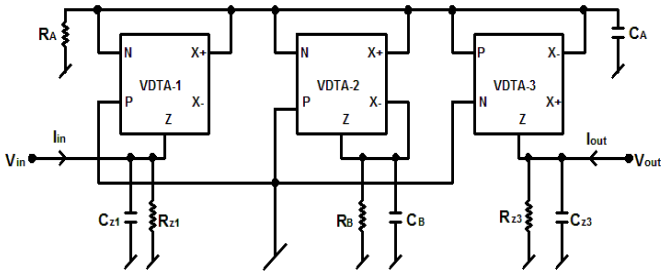


Fig. 5. Proposed configuration including the parasitics of VDTAs

Where

$$R_A = \frac{1}{\frac{1}{R_{n_1}} + \frac{1}{R_{X_1+}} + \frac{1}{R_{n_2}} + \frac{1}{R_{X_2+}} + \frac{1}{R_{p_1}} + \frac{1}{R_{X_3-}}} \quad (13)$$

$$C_A = C_{n_1} + C_{n_2} + C_{p_3} + C_{x_1+} + C_{x_2+} + C_{x_3-} \quad (14)$$

$$R_B = \frac{1}{\frac{1}{R_{z_2}} + \frac{1}{R_{X_2-}}} \quad (15)$$

and

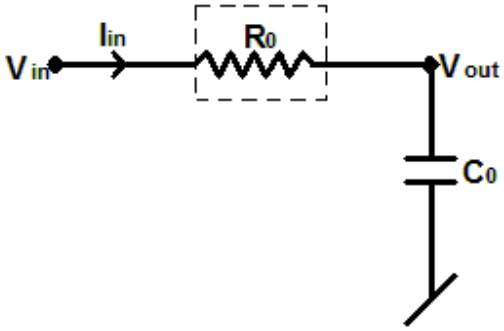
$$C_B = C_{z_2} + C_{x_2-} \quad (16)$$

As the proposed configuration does not have any external passive component, so effects of parasitics cannot be alleviated. Hence, port parasitics of VDTAs will limit the high frequency behaviour of proposed configuration. So, the maximum usable frequency can be found as:

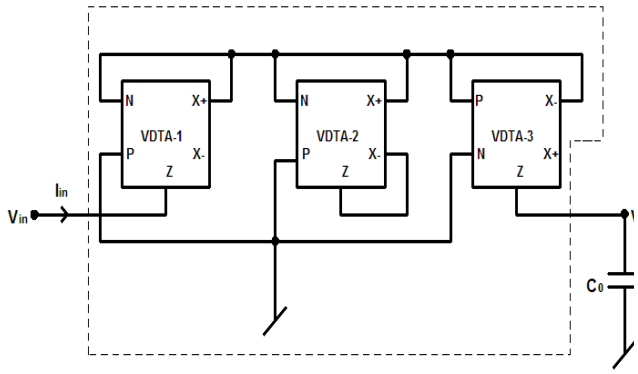
$$\omega_{0_{max}} \langle\langle \min\left\{ \frac{(\frac{1}{R_{n_1}} + \frac{1}{R_{n_2}} + \frac{1}{R_{p_3}} + \frac{1}{R_{x_1+}} + \frac{1}{R_{x_2+}} + \frac{1}{R_{x_3-}})}{(C_{n_1} + C_{n_2} + C_{p_3} + C_{x_1+} + C_{x_2+} + C_{x_3-})}, \frac{1}{R_{z_1} C_{z_1}}, \frac{1}{R_{z_3} C_{z_3}}, \frac{(\frac{1}{R_{z_2}} + \frac{1}{R_{x_2-}})}{(C_{z_2} + C_{x_2-})} \right\} \quad (17)$$

5. Application Examples

The workability of proposed circuit is also verified by low-pass filter design example. The passive RC low-pass filter employing a floating resistor and a grounded capacitor has been shown in Fig. 6(a) and active realization of this low-pass filter using proposed resistor simulator is shown in Fig. 6(b).



(a)



(b)

Fig. 6. Voltage-mode low-pass filter (a) Pasive realization (b) active realiazation employing proposed floating resistance simulator

The voltage mode transfer function obtained from Fig. 6(b) is given by Eq.18, which is low-pass transfer function.

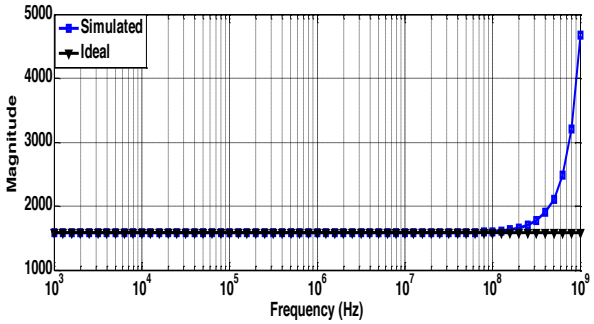
$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+\dfrac{sC_0 g_{m_3}}{g_{m_A} g_{m_B}}} \qquad (18)$$

6. Simulation Results

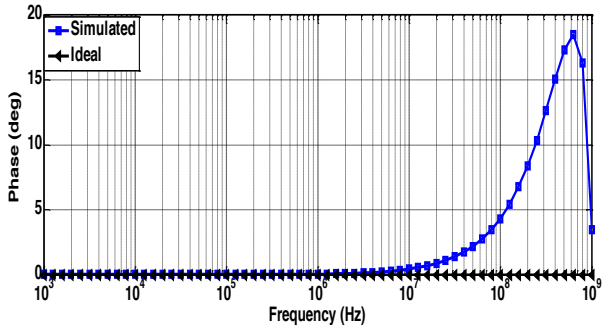
The circuit illustrated in Fig. 3 is tested by SPICE simulations with TSMC 0.18 µm process parameter model. The simulations were performed employing CMOS VDTA (shown in Fig. 2) with supply voltages ±0.9 VDC and bias currents I_{b1}= I_{b2} = I_{b3} = I_{b4} = I_{b5} = I_{b6} = I_{b7} = I_{b8} = I_{b9}= I_{b10} = I_{b11} = I_{b12} = I_b = 150 µA, where I_{b1}, I_{b2}, I_{b3} and I_{b4} are the bias currents of VDTA1, I_{b5}, I_{b6}, I_{b7} and I_{b8} are the bias currents of VDTA2 and I_{b9}, I_{b10}, I_{11} and I_{b12} are the bias currents of VDTA-3. The magnitude and phase response of impedance of proposed simulator have been shown in Fig.8. It is seen from Fig. 8(a) that simulated magnitude response is approximately same as ideal magnitude response up to 286 MHz frequency (simulated resistance value is found 1.566 kΩ while ideal value is 1.571 kΩ. The phase response plots, as shown in Fig. 8(b) clearly indicates that simulated phase response matches the ideal phase response up to 30 MHz frequency. The deviation of simulated responses from ideal responses at high frequencies is due to presence of VDTA parasitics.

To demonstrate the electronic control of proposed configuration, simulations have been performed for different set of bias currents. Fig. 10 illustrated the magnitude responses for I_b = 130 µA and 110 µA. The simulated floating resistance values for I_b = 130µA and 110 µA were found 1.667 kΩ and1.830 kΩ while the ideal values were calculated as 1.689, 1.836 kΩ Hence the deviation between simulated values and ideal values is not more than 1.5% in limited frequency region.

The low-pass filter shown in Fig. 6(b) is also simulated using CMOS VDTA with supply voltage of ±0.9 VDC. The value of capacitor C_0 is chosen as 0.1nF. The SPICE simulated frequency responses of this filters is shown in Fig. 9.



(a)



(b)

Fig. 7. Frequency reponses (a) Magnitude response (b) Phase response

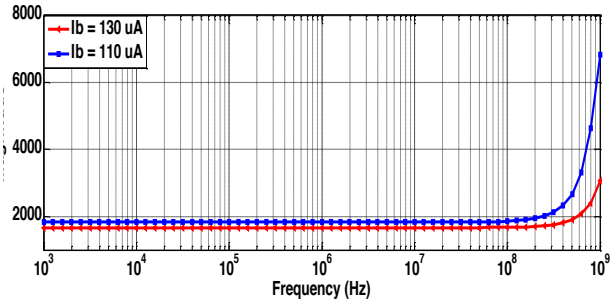


Fig. 8. Demonstration of elecronic control

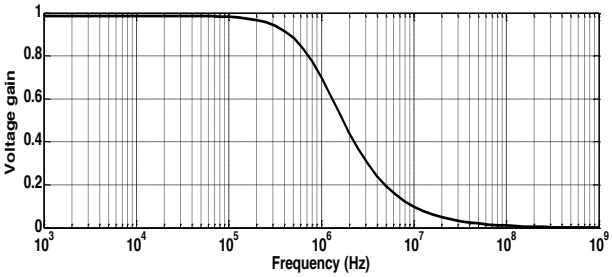


Fig. 9. Frequency response of low-pass filter shown in Fig. 6(b)

7. Conclusion

A new purely active floating resistor simulator employing three VDTAs has been presented. To the best knowledge of authors there is no purely active floating resistor simulator employing VDTA(s) has been available in literature. The proposed configuration enjoys electronically tunable resistance with low sensitivity indexes. The effects of non-idealities and parasitics of VDTA also have been investigated in proposed circuit. The application of proposed resistor simulator in designing of a low pass filter has been proposed and verified. The mathematical analysis has been verified by SPICE simulations with TSMC 0.18µm CMOS process parameters.

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