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Research Article

Reversible Squaring Circuit for Low Power Digital Signal Processing

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Abstract

With the high demand of low power digital systems, energy dissipation in the digital system is one of the limiting factors. Reversible logic is one of the alternate to reduce heat/energy dissipation in the digital circuits and have a very significant importance in bioinformatics, optical information processing, CMOS design etc. In this paper the authors propose the design of new 2- bit binary Squaring circuit used in most of the digital signal processing hardware using Feynman & MUX gate. The proposed squaring circuit having less garbage outputs, constant inputs, Quantum cost and Total logical calculation i.e. less delay as compared to the traditional method of squaring operation by reversible multiplier. The simulating results and quantized results are also shown in the paper which shows the greatest improvement in the design against the previous methodology.

Keywords: Reversible logic, quantum cost, garbage outputs, Total logical calculation, constant inputs, MUX gate, Feynman gate.

1. Introduction

Today's human's life cannot be imagine without the digital electronic systems. There are endless examples of electronic systems hardware can be found all around us: Radios, computer systems, compact displayer, telephone systems, video games, and microprocessor and digital watches- the list seems to be going forever! This rapid growth in the electronic industries also forces to designer to struggle for the designing of the efficient low power digital systems because the power loss and the energy loss is one of the limiting factor in the digital systems [10]. The logic design and the switches are the two main contributor of energy or power loss in the digital systems [4][5][7][9]. Even if Rolf Landauer in 1961 predicted that the irreversible logical computation device designed by the conventional approach having an entropy gain is S= K ln W. where W=2N, the number of states [1]. The entropy of a system could be defined as the ratio of heat to the temperature at which the calculation is performed. So, by this we get the expression for the energy or heat dissipation i.e. equal to the KT ln 2[1][4-11]. Where K is the Boltzmann's constant equal to $1.3806505 \times 10^{-23}$ $m^2kg^2k^{-1}$(J/K) and T is the temp. At which the logical computation is performed. This dissipated energy is directly correlated the number of lost bits [2]. On the other hand, due to the switching action in the conventional (irreversible) digital systems implemented by modern CMOS technology consumes energy Esig = ½ CV2 which is the energy of the voltage-coded signal [7].

Furthermore, the co-founder of Intel (Gordon Moore) stated that the processing power will double every 18 months, will stop functioning in the year 2010- 2020 called Moore's Law[4]. So, resultantly a new alternative approach of designing the digital system has been arose with the motto of reducing energy dissipation and subsequently reducing the entropy increase called Reversible Logic design. In 1973, C.H. Bennet showed that if the systems designed by the reversible designing approach instead of the conventional approach dissipated less heat or ideally no heat[2][3].

Reversible logics use the charge recovery process to save energy. These are the logic which does not loose information. The reversible circuits are designed by the special logical gates called reversible gates. Reversible logic structure posses the property of one to one mapping between the inputs and output state[4[[5][8][9] for the designing of the reversible logic circuits there are two main conditions has to be follows strictly[10]:

Fan-Out is not permitted
Feedback is not permitted

These reversible gates are having the very vast applications in the field of quantum computing, bioinformatics, CMOS designing optical computing etc.[9]

1.1 Motivation

The Arithmetic calculation is the one of the important part of any of the digital hardware [11]. The squaring calculation has its own advantages in different field like digital signal processing: Convolution, deconvolution, cryptography etc. where numbers of times we have to calculate fast square of the number [12-13]. In order to calculate the square of the binary **numbers**, there are number of faster reversible multiplier by which we calculate the square of the numbers [12]. The reversible multiplier proposes in the literature are generally based on the recursive method [13]. But, to designing of any of the digital hardware the circuit complexity is one of the important measures which directly correlate with the delay [4]. So, the main motivation behind this work is to investigate the implementation of the efficient

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and low power squaring circuit architecture for the digital hardware industries. In this paper, we are proposing a reversible squaring circuit for the fast squaring calculation instead of using multiplier for the squaring which increases the complexity and the delay in the circuit. The proposed circuit is much effective and having less complexity and the less delay as compared to multiplier used for the squaring. For the simplicity for the readers, we are proposing a 2 ×2 squaring circuit which can perform two bit square operation and showing the results that this proposed architecture is much efficient as compare to the square operation performs by the reversible multiplier.

This paper is organizes in such a manner that the section 2 will provide the basic information about the reversible logics. The logic configuration of the MUX gate, MUX gate as a half adder and the Feynman gate is describes in this section. Section3 will give the proposed architecture of the reversible squaring circuit with the traditional reversible multiplier. The section 4 will give the simulation results and the quantized results for the proposed architecture against the reversible multiplier for squaring computation. Last section will provide the conclusion about the paper.

1. Background of the Reversible Logics

The Reversible gates are the gates which have the same numbers of inputs and outputs and for each input pattern there must be a unique pattern. Thus, the reversible logics has one to one mapping between their inputs and outputs[3]. So, to represent the N × N reversible gate,

IV = (I1, I2, I3……, IN)

Ov = (O1, O2,O3……, ON)

Where Iv and Ov are the input and output vectors respectively. The conventional logic gates are irreversible gate because the input and the output vector are not same. The conventional inverter is the reversible gate[7].

For the reversibility in a circuit, not only logical but also be physical reversibility must be present. The physically reversibility means, the systems must be able to run backward i.e. the input can be retrievable by the output [6]. Along with the design conditions, there are some main measures of the reversible logics. However, the main parameter in the convention or irreversible designs is numbers of logic gate used. Unlike of convention logics, the reversible gate has different parameters as follows[8][9]:

QC (Quantum cost) [6]: The number of reversible gates (1×1 or 2×2) to realize the circuit is known as quantum cost,
(CI) Constant inputs [6]: The number of inputs that are kept constant (0 or 1) for synthesis the given functions,
GO (Garbage outputs) [6]: The number of outputs that are not primary is known as Garbage outputs
Total logical calculation (T): Total logical calculation is the count of the XOR, AND, NOT logic in the output circuit [4].

There are several reversible logic gates have been proposed in the last years such as: Feynman gate [4], Fredkin gate [8], Peres gate [9] Toffolli gate [3], Mux gate [5] etc. Here we are reviewing the two gates i.e. Feynman, and MUX gate because these gates are used in the targeted design.

2.1 MUX gate [5]:

Fig.1 shows the pictorial representation of 3×3 reversible gate called MUX (MG) gate. It is a conservative gate having three inputs (A, B, C) and three outputs (P, Q, R). The outputs are defined by P=A, Q=A XOR B XOR C and R= A'C XOR AB. The hamming weight of its input vector is same as the hamming weight of its output vector and its Quantum cost is 4.

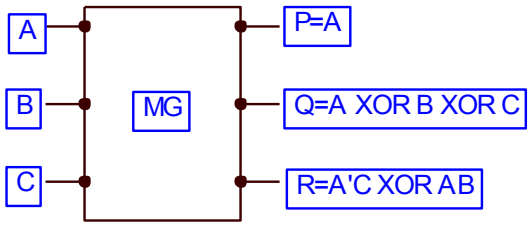

Fig.1. 3×3 MUX gate

2.1.1 MUX gate as Half Adder

The structure of MUX gate as Half adder is shown in the fig1.1. If we provide '0' at third input C then the output Q will provide the Sum of the half adder and R will provide the AND combination of first & second input or Carry output for the half adder.

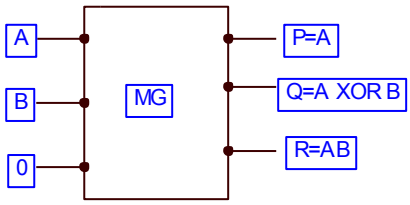

Fig1.1. MUX gate as Half Adder

2.2 Feynman Gate [4]

Fig.2 shows the 2×2 reversible gate called Feynman gate. Feynman gate is also recognized as controlled- not gate (CNOT). It has two inputs (A, B) and two outputs (P, Q). The outputs are defined by P=A, Q=A XOR B .This gate can be used to copy a signal. Since fan-out is not allowed in reversible logic circuits, the Feynman gate is used as the fan-out gate to copy a signal. Quantum cost of a Feynman gate is 1.

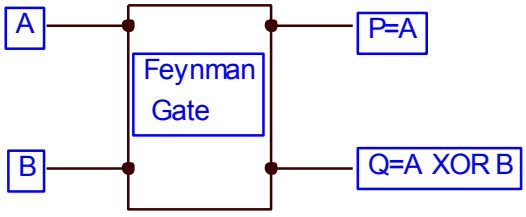

Fig.2. 2×2Feynman gate structure

2.2.1 Feynman gate as Data Copier & as NOT gate[4]

The structure of Feynman gate as Data Copier & as NOT gate is shown in the fig 2.1 & 2.2 resp.If we provide '0' at second input B then the output Q will provide the copy of

first input and if we If we provide '1' at second input B then the output Q will provide the complement of the first input.

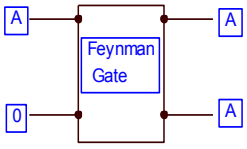

Fig 2.1. Feynman gate as Data copier

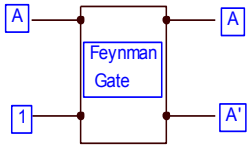

Fig.2.2 Feynman gate as NOT gate

2. Proposed Architecture of New Reversible Squaring Circuit

The Multiplication of the binary number is the basically a recursive addition of the bits[8]. The reversible multiplier which was discussed in the literature is used for the squaring of the binary numbers. But in this paper, by seeing the use of the binary square calculation in the different field, we present the design of the reversible squaring circuit with the aim of the optimizing hardware complexity to make it more economical in terms of garbage outputs, constant inputs and total logical calculations without losing the bits.

3.1 Design of 2 × 2 reversible binary multiplier

The traditional reversible multiplier is used for the squaring calculation of the bits.The fig.3(a) and fig 3(b) Shows the 2 × 2 reversible binary multiplier Block diagram and the gate level logical diagram by using the MUX gate. In this we uses feynman gate for copying the signal and avoiding the feedback.

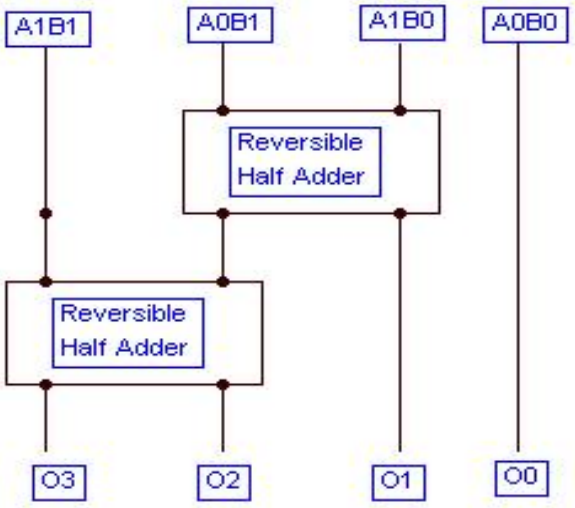

Fig.3(a) 2 × 2 reversible binary multiplier Block diagram

In this, we have two bits number represented A1A0 & B1B0 then there is a ANDing of A0B0, A1B0, A0B, A1B1. The Result O0 will be same as A0B0 and the O1 will be addition of A1B0 and A0B1 through half adder , O2 will be the addition of previous carry and the A0B1 through half adder and the O3 will be the carry bit from that adder. This process can be demonstrated as:

O0 (1-bit) = A0B0
O1 (1-bit) A1B0 + A0B1
O2 (1-bit) = A1B1+ O1+ C1 (carry from O1)
O3 (1-bit) = C2 (carry from O2)

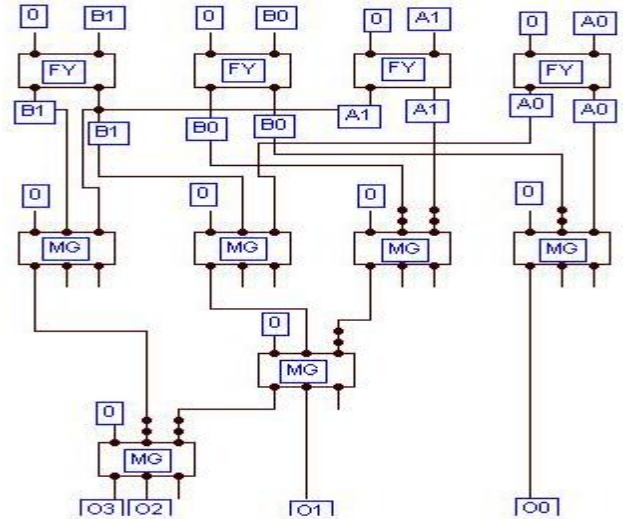

Fig 3(b) gate level logical diagram by using the MUX gate

3.2 Design of 2 × 2 reversible binary multiplier

The fig.4(a) & fig 4(b) shows the 2 × 2 reversible binary squaring circuit block diagram and gate level logical diagram by Feynman and MUX gate.

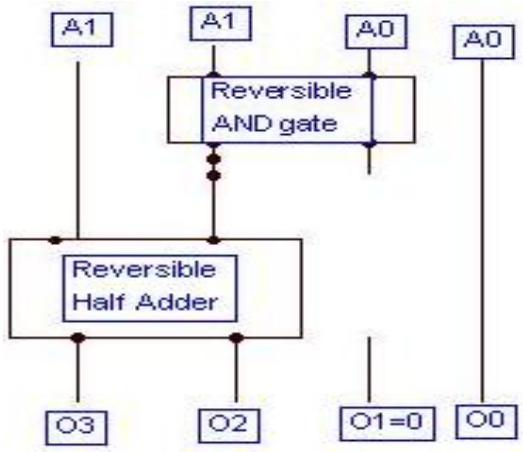

Fig.4(a) 2 × 2 reversible binary squaring circuit block diagram

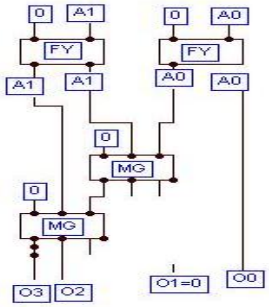

Fig 4(b). Gate level logical diagram

3. Results

4.1 Simulation Results

The propose Reversible Squaring Circuit architecture shown in previous section is implemented and resulted by using VHDL and simulated in Xilinx ISE8.2i. For the designing of the reversible squaring circuit we use the structural and behavioral modeling. The VHDL codes for the MUX gate and Feynman gate is written in behavioral modeling and these gate are connected to each other by structural modeling (port mapping)[14]. The simulated results of the reversible squaring circuit can be seen in fig.5

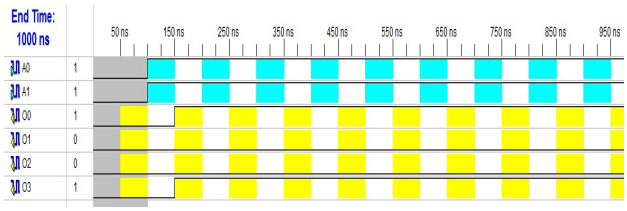

Fig.5. Simulated results of the reversible squaring circuit

Table 1. Design Summery

Device Utilization Parameters (Spartan 3)	2-bit Squaring By 2×2 rev Multiplier	Proposed 2-bit rev Squaring Circuit
Number of 4 I/p LUT's	4/3840	2/3840
Number of slices	2/1920	1/1920
Number of bounded IOBs	8/173	6/173

4.2 Quantized evaluation of parameters in proposed Reversible Squaring circuit

In case of reversible logic the important parameters are total logical calculations, No. of gate used, Garbage outputs, constant inputs and Quantum cost. These are calculated for existing binary multiplier and for proposed squaring circuit for the squaring operation. The comparative findings are shown in table 2.

4.2.1Total Logical calculation (T)

Assuming

α = A two input XOR gate calculation
β = A two input AND gate calculation
δ = A NOT gate calculation
T = Total logical calculation

The Total logical calculation is the count of the XOR, AND, NOT logic in the output circuit. For example MUX gate has three XOR gate and two AND gate and one NOT gate in the output expression. Therefore $T_{(M)} = 3\alpha+2\beta+\delta$.

In the binary 2×2 reversible multiplier for the squaring calculation, the total number of logical calculation T is: $T= 6\times (3\alpha+2\beta+\delta)$(for MUX gate)+ $4\times1\alpha$(for Feynman gate) = $22\alpha + 12\beta+6\delta$ and for proposed 2-bit reversible squaring circuit , the total logical calculation $T = 2\times (3\alpha+2\beta+\delta)$(for MUX gate)+ $2\times1\alpha$(for Feynman gate) = $8\alpha + 4\beta+2\delta$.

So, by this calculation the total logical calculation for the targeted number is less for the proposed design

4.2.2 Number of Reversible Gates Used

As we have discussed previously, the delay in the digital hardware is one of the limiting factor and this factor is directly linked with the uses of the number of gates. So, the number of reversible gates for the binary 2×2 reversible multiplier for the squaring calculation is 4 Feynman gates and 6 MUX gates. But the number of reversible gates for the proposed 2-bit reversible squaring circuit is 2 Feynman gates and 2 MUX gates.

4.2.3 Constant Inputs

The number of inputs that are kept constant (0 or 1) for synthesis the given functions are constant inputs. The CI produces the GO. So, it must be less for a pretty design of the reversible circuit for producing secondary outputs (GO). The number of constant inputs for the binary 2×2 reversible multiplier for the squaring calculation is 10. But the number of constant inputs for the proposed 2-bit reversible squaring circuit 3

4.2.4 Garbage Outputs

The garbage outputs are the outputs which are not primarily used or for a better designing of the reversible circuit, the garbage outputs kept less as possible. So, the number of garbage outputs for the binary 2×2 reversible multiplier for the squaring calculation is 10. But the number of garbage outputs for the proposed 2-bit reversible squaring circuit 3

4.2.5 Quantum Cost

As we have used Mux gate whose quantum cost is 4 and for Feynman gate the quantum cost is 1. So, if there is 'm' number of MUX gates used in the structure then complete quantum cost becomes 4m and if there is 'f' number of Feynman gates used in the structure then complete quantum cost becomes 1f. So, quantum cost for the binary 2×2 reversible multiplier for the squaring calculation is 4f+6m. But the quantum cost for the proposed 2-bit reversible squaring circuit is 2f+2m.

Table 2. Parameters comparison

Parameters	2-bit Squaring By 2×2 rev Multiplier	Proposed 2-bit rev Squaring Circuit
Number of Reversible Gates	4 Feynman 6 MUX	2 Feynman 2 MUX
GO(Garbage ouputs)	10	3
CI (Constant Inputs)	10	3
QC(Quantum Cost)	4f+6m =28	2f+2m =9
T(Total Logical Calculation)	$22\alpha + 12\beta+6\delta$	$8\alpha + 4\beta+2\delta$.

Where f = No. of Feynman gates.
m = No. of Mux gates

This is the demonstration of the 2-bit squaring circuit. For the higher bit quaking like for the 4- bit we have to use only two 2- bit reversible squaring circuit and one 2 ×2 reversible multiplier instead of using four 2 ×2 reversible multiplier and likewise for the 8-bit we have to use only two 4- bit reversible squaring circuit and one 4 bit reversible multiplier.

4. Conclusions

Squaring operation in the different field having their own importance. The fast and efficient squaring calculation is one of the demands in the convolution, de-convolution or in other part of DSP. In this paper we emphasis on using proposed hardware design low power Squaring circuit for digital signal processing instead of multiplier for the squaring operation. The proposed squaring circuit is much cost efficient with the lesser garbage outputs, constant inputs and hardware complexity as compared .The simulated results of the proposed design is also shown which are completely verified and correct in all sense. The design summery is also shows the there is a saving of 50% in the 4 I/p LUTs and in number of slices with the 25% in the bounded IOBs. Which shows that the proposed design have high speed. So, the proposed design of squaring circuit is highly efficient and we expect that, this work will definitely provide a new approach for design of low power and speedy squaring computing hardware for DSP's.

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