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Research Article

Crystalline silicon cells and modules in present photovoltaics

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Abstract

Impressive progress in PV technology over the past thirty years is evident from the lowering costs, the rising efficiency and the great improvements in system reliability and yield. Yearly growth rates in the last decade (2003-2013) were on an average higher than 40%, and the global cumulative PV power installed reached 140 GWp in 2013 and photovoltaic power installed in 2013 overcome 30 GWp. The workhorse of present photovoltaics is crystalline silicon technology. Basic principles of photovoltaic cell physics and technology have been demonstrated on fabrication of crystalline silicon cells and modules, also new prospective technologies. Differences between technologies are discussed and present domination of crystalline silicon technology is explained. The aim is to give information important for understanding basic problems of physics, construction and manufacturing photovoltaic cells and modules.

Keywords: photovoltaic module, crystalline silicon cells, crystalline silicon modules, fabrication

1. Introduction

At the present time, photovoltaics is one of the most dynamically growing industries [1]. Impressive progress in PV technology over the past thirty years is evident from the lowering costs, the rising efficiency and the great improvements in system reliability and yield. Yearly growth rates in the last decade (2003-2013) were on an average higher than 40%, and the global cumulative PV power installed reached 140 GW_p in 2013 [2], as demonstrated in Fig.1. Photovoltaic installations in individual regions in the end of the year 2012 are shown in Fig.2.

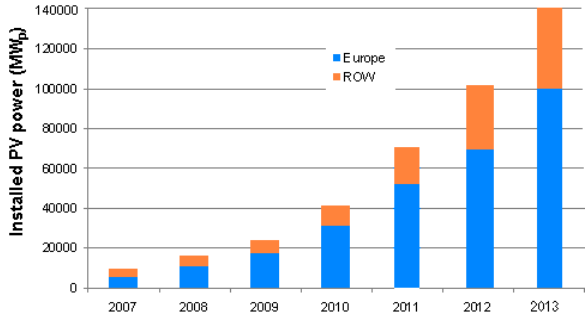
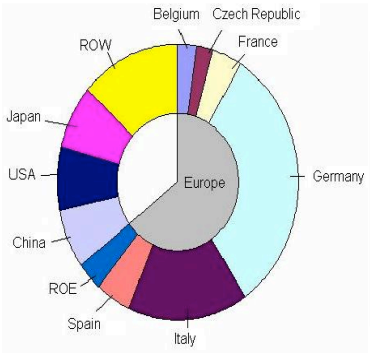


Fig.1. Historical development of World cumulative PV power installed in main geographies

As follows from Fig.2, the most PV installations were realized in Europe, where the yearly irradiance varies between 800 and 1800 kWh/m^2. Despite relatively low irradiance level (from 900 to 1300 kWh/m^2), Germany has become the leading country in photovoltaic installation due to introduction of a feed-in tariff for on-grid systems in 2000. This initiated a very fast growth of photovoltaic installation in the EU, where already in 2007 the level of 3 GW_p was reached, the level of 50 GW_p was reached in 2011 and the photovoltaic installations in 2013 reached 73 GW_p that is more than 50% of the global cumulative PV power installations.



country	installed capacity (GW_p)
Belgium	2,6
Czech Republic	2
France	3,9
Germany	32,1
Italy	16
Spain	4,7
ROE	3,3
China	7,1
USA	7,6
Japan	7,5
ROW	13,2

Fig.2. Accumulated PV installations in the World in 2012 (102 GW_p)

The most of installed power (over 90%) are on-grid systems, where the energy cost is still higher than in the case of fossil energy sources (standard power plants) and spreading the photovoltaic on-grid power stations has been done mostly by using feed-in tariff. Therefore, the most important task in previous years has been decreasing cost of photovoltaic modules below 1 €/W_p, that means decreasing cost of the PV system below 2 €/W_p with a target to get the PV system cost close to 1 €/W_p [1]. Continuous progress in decreasing the final price of the energy produced from photovoltaic is based on reduction of the production cost of solar cells, keeping the high production yield as well as on enhancing the cell and module efficiency [3], [4], to get closer to the dynamic grid parity [4].

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Since 1970, silicon is the most important material for photovoltaic cell and module fabrication (about 90% of all PV modules are made from silicon). Despite four decades of research and manufacturing, scientists and engineers are still finding ways to improve the performance of Si-wafer photovoltaics and ways of reducing the cost. The present state of art and future trends in silicon wafer based technology will be discussed in following paragraphs.

2. Photovoltaic cells and module physics and construction

Photovoltaic cells and modules have been discussed in details in many publications (e.g. [6], [7], [8], [9], [9], [10], [11]). The basic function of a photovoltaic cell can be described using a structure shown in Fig.3. Photons with energy *hv* higher than band-gap W_g are in the illuminated area absorbed generating electron-hole pairs, which diffuse towards the region with build-in electric field (e.g. PN junction or heterojunction) situated in a distance x_j below the illuminated surface. Due to a strong electric field, all holes in N-type region reaching the space charge region boundary are drifted into the P-type region and all electrons reaching the space charge region are drifted into the N-type region. This way, the P-type region is charged positively, the N-type region is charged negatively, and between both regions is a potential difference. This voltage is capable of driving a current through an external circuit and thereby producing useful work on a load. Crystalline silicon has relatively low absorption coefficient for wavelength in infrared part of solar spectra. Therefore, a thickness of the base material should be more than 100 μm for an efficient solar cell, and starting material should be a wafer fabricated from crystalline silicon, while in the case of "direct semiconductors", where the absorption coefficient increases very quickly with photon energy, the base thickness can be bellow 3 μm and the cell can be realized as a thin layer on a suitable substrate.

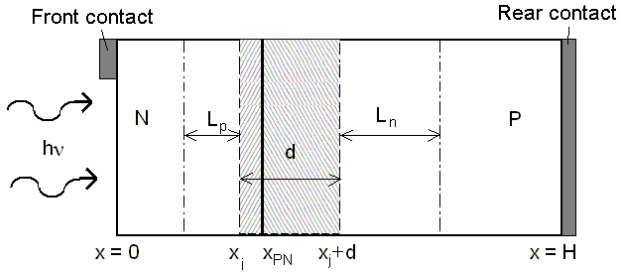

Fig.3. PN junction solar cell structure

Carriers generated by incident light and collected by the junction space charge region create photovoltaic current of the density J_{FV}. A part of generated carriers recombines before reaching the space charge region due to a limited carrier lifetime τ. The photovoltaic current density can be expressed by

$$J_{PV} = q\int_0^H G(x)dx - q\int_0^H \frac{\Delta n}{\tau}dx - J_{sr}(0) - J_{sr}(H), \qquad (1)$$

where $J_{sr(0)}$ represents the surface recombination at x = 0 and $J_{sr(H)}$ represents the surface recombination at $x = H$.

From the viewpoint of solar energy conversion in number of generated carriers, this depends strongly on type of semiconductor (band gap, band structure). The maximum efficiency of conversion in dependence on band gap with respect to solar spectrum AM 1,5 is shown in Fig.4. From that it is possible to evaluate suitability of different semiconductor materials for solar cell fabrication.

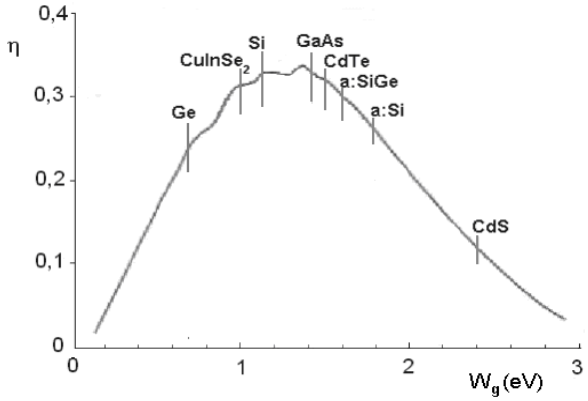

Fig.4. Maximum conversion efficiency in dependence on band gap (spectrum AM 1.5)

The PN junction is biased by the light-induced voltage in the forward direction and the maximum voltage is limited by the forward I-V characteristic of the PN junction. Then, the solar cell can be modelled as a PV current generator with a in parallel connected diode. Imperfections of the PN junction result in a parallel resistance R_p across the junction. As the current of carriers collected by the PN junction flows to output contacts through material with a finite resistance, any solar cell has a series resistance R_s between the PN junction and output contacts. The equivalent circuit of a solar cell is shown in Fig.5.

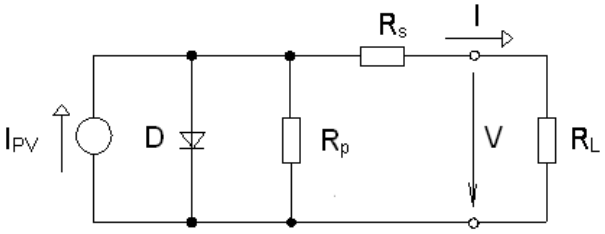

Fig.5. An equivalent circuit of a solar cell

If V is the output voltage, I is the output current and R_s is the series resistance, across the PN junction is the voltage $V + IR_s$ forward biasing the diode. A part of photo-generated current flows through the diode and through the parallel resistance R_p. Therefore, if A is the total solar cell area, the output current is in a simple approximation

$$I = A_{ill}J_{PV} - I_{01}\left[\exp\left(q\frac{V + R_sI}{\zeta\, kT}\right) - 1\right] - \frac{V + R_sI}{R_p}, \qquad (2)$$

where J_{PV} is density of current generated in the volume of the cell structure, $A_{ill} \le A$ is the illuminated area of the cell, I_{01} is the reverse current of non irradiated diode and ζ is so called the diode factor ($1 \le \zeta \le 2$). The I-V characteristic is schematically shown in Fig.6. The important points of the I-

V characteristic can be derived from (2). The open circuit voltage V_{OC} can be found from (2) for $I = 0$. If the parallel resistance R_p is high, the open circuit voltage

$$V_{OC} = \frac{\xi\, kT}{q} \ln \frac{I_{PV}}{I_0}. \quad (3)$$

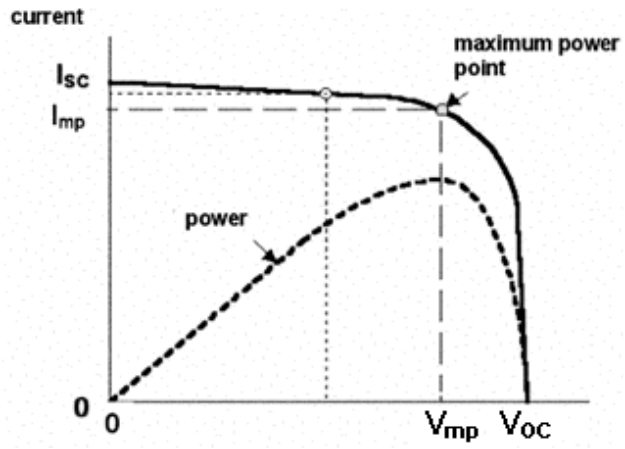

Fig.6. Solar cell characteristics

From (3) follows, that the quality of collecting junction represented by the diode factor ζ and dark reverse current I_0 influence the open circuit voltage V_{OC}, as demonstrated in Fig.7. Imperfections of the junction represented by the parallel resistance R_p result also in a decrease of V_{OC}. The short circuit current I_{SC} can be obtained from (2) for $V = 0$. A typical value of J_{SC} for commercial crystalline silicon solar cells is about 35 mA/cm^2 under standard testing conditions (e.g. irradiation 1000 W/cm^2, spectrum AM1.5, temperature 25°C). The short circuit current I_{SC} decreases with increasing series resistance R_s. In an ideal case ($R_s = 0$ and $R_p \rightarrow \infty$), the fill factor $FF \approx 0.89$. With increasing R_s (or decreasing R_p) both maximum power $I_{mp}V_{mp}$ and fill factor FF decrease and consequently, efficiency decreases. The influence of series resistance R_s on PV cell efficiency in dependence on irradiance [13] is schematically shown in Fig.8.

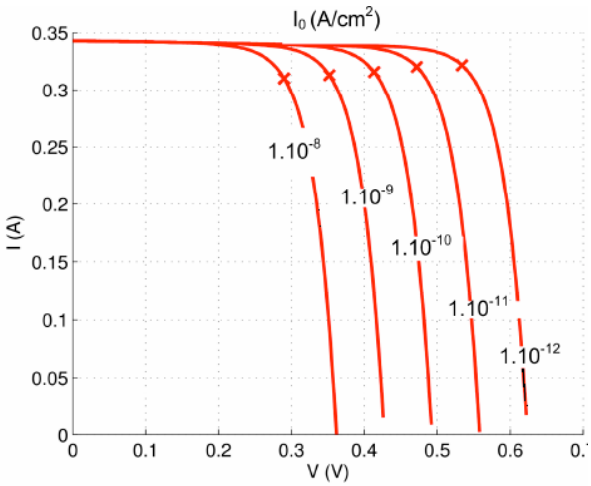

Fig.7. The influence of the dark reverse current I_0 on the open circuit voltage V_{OC}

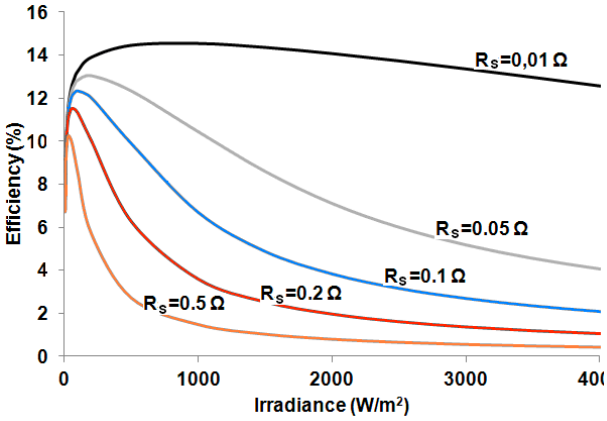

Fig.8. The influence of series resistance R_s on PV cell efficiency in dependence on irradiance

Parameters of PV cells depend on temperature. As the dark reverse current I_0 increases with temperature, $I_0 \sim T^3 exp(-W_g/kT)$, from (3) follows that V_{OC} decreases significantly with temperature (for silicon cells the decrease of V_{OC} is about 0.4%/K), while short circuit current I_{SC} only very slowly increases with temperature. Consequently, the other parameters, maximum power, fill factor and efficiency, also decrease significantly with increasing temperature. An example of the cell efficiency dependence on temperature and irradiance (standard c-Si cell) is shown in Fig.9.

T o obtain a high efficiency of solar cells, the construction and fabricated technology should be prepared in the way to maximise carrier generation and minimise all kind of losses in the solar cell structure, as schematically shown in Fig.10. For obtaining high voltage V_{OC}, the cell should have high I_{PV} and low I_0. For obtaining high I_{PV}, from (1) follows that it is necessary to maximise carrier generation and minimise losses by both bulk and surface recombination for spectral distribution of solar radiation. It is also very important minimise optical losses decreasing surface reflectivity. As follows from (2), the cell construction and technology should keep low R_s by optimising contact pattern to minimise electrical losses.

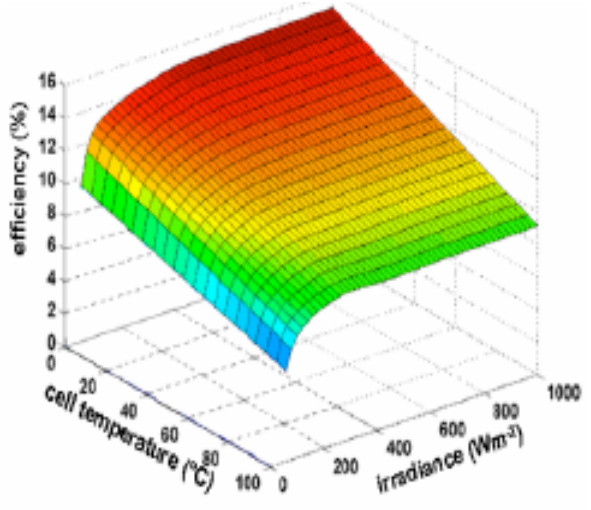

Fig.9. C-Si cell efficiency dependence on temperature and irradiance

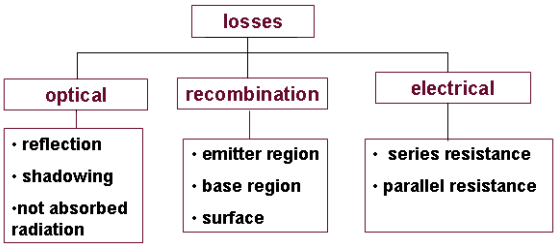

Fig.10. Possible losses in solar cell structures

As the voltage of a single solar cell is low (usually less than 1V), several of them must be connected in series to make a practical generator. A number of cells are usually connected in series and encapsulated in so called modules. The module is the building unit for photovoltaic generator and it is the real PV product at the market. The I-V characteristics of a PV module can be derived from the scheme in Fig.11. Usually, the scheme is simplified using equivalent circuit consisting of a number of current generators in series clamped with the same number of in series connected diodes. Series resistances of in series connected individual cells are replaced with an equivalent module series resistance R_s' and parallel resistances R_p'. In this approach, the module I-V characteristic is formally similar to (2). For the module characteristic it is possible to define the same parameters as for photovoltaic cells, i.e. short circuit current I_{SC}, open circuit voltage V_{OC}, maximum power $P_{m,}$ voltage V_{mp} and current I_{mp} in the maximum power point, fill factor FF and efficiency η. It is very important all in series connected cells have the same I_{mp} to obtain high module efficiency.

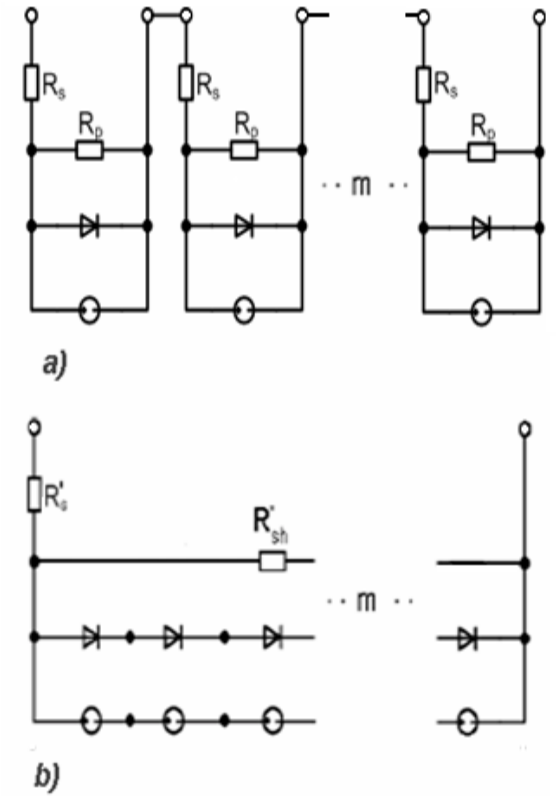

Fig.11. An equivalent circuit of a PV module

3. Crystalline Silicon (wafer based) technology

3.1. Cell Fabrication

Crystalline silicon photovoltaic cells are usually fabricated from boron doped P-type Si. The boron dopant has a relatively high segregation coefficient of 0.8 [14] that results in low resistivity variations along the entire length of the boule [15],[16] that increases yield of crystalline silicon material with defined parameters. The starting wafers (monocrystalline or multicrystalline) of thickness in the range of 150-250 μm are prepared from square shaped rods (monocrystalline or multicrystalline) by wire cutting [17],[18].

In the manufacture of (standard) solar cells 6 or more steps are required in succession typically: texturing of the surface, doping, diffusion, removal of the oxide, antireflection coating, metallisation and firing [9],[11],[12]. In the end of the process the cell efficiency and other parameters are measured (under standard testing conditions) and cells are sorted by the current I_{mp}. Standard cell structure is shown in Fig.12.

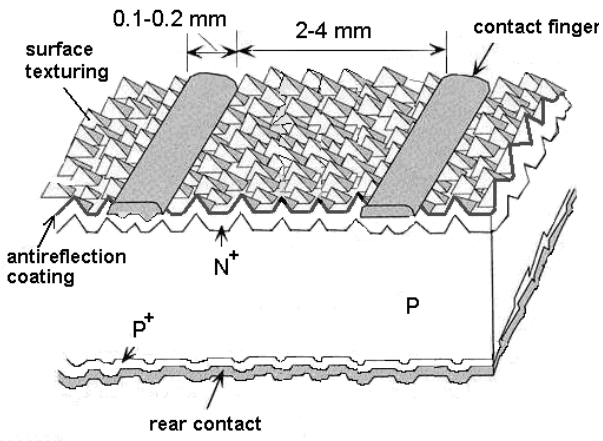

Fig.12. Standard crystalline silicon cell structure

Every technological step has a direct or indirect influence on the cell's performance. Some steps influence each other, like diffusion and the material quality (decrease of bulk recombination by gettering), texturing and diffusion (surface cleaning) or the antireflection coating by SiN:H (hydrogen passivation of both front surface and grain boundaries in case of the multicrystalline material). The contact grid on the front surface has usually so called H-shape consisting from a number of thin equidistant fingers collecting generated current and cross connected with two or three relatively wide busbars, as shown in Fig.13. The contact grid is realised by print screening the phosphorous-doped silver paste on N-type layer covered with silicon nitride layer. On the back surface, a layer of the paste containing silver and aluminium is deposited by print screening. The ohmic contact is formed by firing at over 800°C (lead borosilicate glass frit contained within the Ag paste etches through the SiNx:H layer to form a direct bond and electrical contact with the underlying N^+ emitter region, Al in paste on the rear of the cell forms a good contact with the P-type Si). Standard cell efficiency is about 15- 19 % for

monocrystalline PV cells and 14-18 % for multicrystalline PV cells. This design has been proved to be ideal in the overall costs.

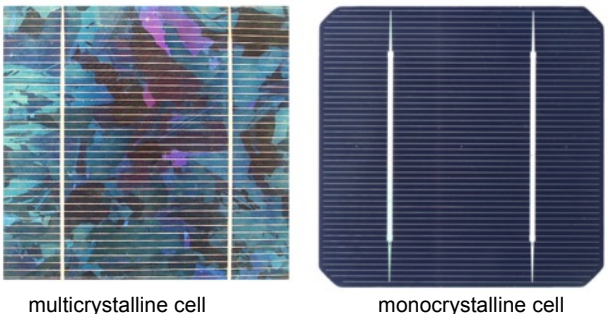

Fig.13. The H-shape contact grid on the front surface of cells

Improvements in crystalline silicon technology (a higher starting wafer quality, decrease of surface recombination and thinning the wafer) result in increase of efficiency and decrease in material consumption, as is indicated in Fig.14.

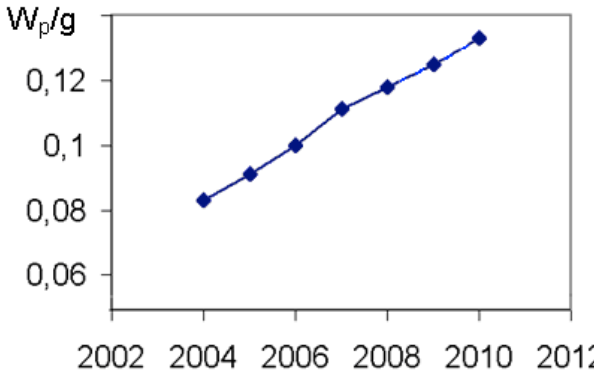

Fig.14. Development of peak power produced from 1g of crystalline Si

One of tools used for improvements of c-Si photovoltaic cells fabricated from starting P-type material is using selective emitter decreasing both Auger recombination losses in the high doped N^+ emitter layer and contact resistance [19]. This construction is based on a heavily doped emitter N^+ region that is narrowly focused at the point of contact between Si and the front side metal, in addition to a less doped N-type emitter region over the entire wafer front surface. The overall expected result when employing such a design is a lowered value in the overall J_0, as well as a slight increase of the J_{SC} (from Eq.(1) follows that lower recombination in the N-region results in an increase of the J_{PV}) of the cell, which results in a correspondingly higher V_{OC}. Cells of this type can be realised by several ways. The most popular seems the forming a pattern of trenches in the silicon wafer with a laser ablation, as demonstrated in Fig.15. The laser groove is envisioned to be advantageous for either the printed dopant paste or aqueous-based approaches to emitter drive-in, often using the laser-assisted doping. The contact grid may be realised by a precisely aligned screen printing Ag paste or (more advantageously), using electroless plating the N^+ region in the groove with a thin nickel layer with following electroplating with a copper alloy [20], as demonstrated in Fig.16. The electroplated Cu contact layer may be used for decreasing Ag consumption for cell fabrication. The technology allows produce much narrower grid line widths (of around 30–50 μm) and reduce losses due to shadowing of light from the front side metal contacts.

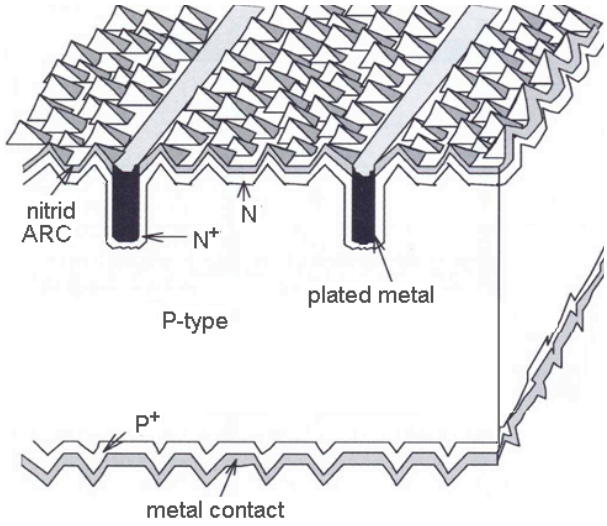

Fig.15. The selective emitter in trenches prepared by a laser ablation

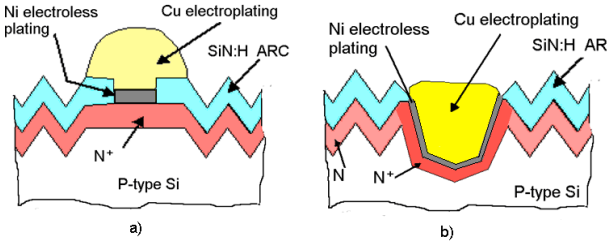

Fig.16. The plated contact structure

Reducing losses due to shadowing from contact bus bars on the front side of cells can be reached also by connecting the contact grid (consisting from narrow lines) to bus bars on the rear of cells by a limited number of holes through the wafer (the so-called metal wrap through – MTW technology). The structure is demonstrated in Fig.17. Transferring the bus bars to the rear surface, the front shading losses can be reduced and rear bus bar contact technology makes easier the module fabrication [21]. In comparison with the standard technology, the MWT technology needs only two additional steps: laser via drilling and rear contact isolation.

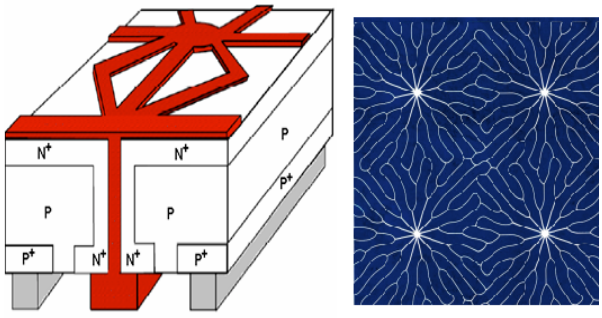

Fig.17. The MWT solar cells

These technologies (selective emitter, surface and grain boundary passivation, and MWT) can be used in the case of

cells fabricated from starting P-type material, both monocrystalline and multicrystalline and allow to reach cell efficiency close to 20%. Unfortunately, boron doped material prepared by Czochralski method or block casting contain the metastable boron–oxygen complexes that lead to the carrier lifetime degradation (after illumination it will rapidly decay from the hundreds of microseconds to the tens of microseconds [15]) and, in consequence, it limits the cell efficiency by 20%.

Pophorous doped N-type silicon wafers retain lifetimes on the order of milliseconds under the same stresses [22], [23] and therefore it can be used as a starting material for high efficient solar cells. Phosphorous has a lower segregation coefficient than boron (0.35) that causes about 25% yield loss in comparison with boron doped P-type wafers. The PN junction is formed by boron diffusion [24]. A disadvantage of this technology is that for surface passivation there must be used a layer of thermally grown SiO_2, on which is deposited a thin layer of SiN_x:H or TiO_2 to form effective antireflection coating. This technology is also not compatible with multicrystalline material because it does not tolerate temperatures above 900 ° C [12].

The high carrier lifetime in N-type starting wafers allows localization of current collecting contacts of both polarities exclusively on the rear side of the PV cell (IBC – Interdigitated Back Contact). Front contact shading area typically occupies up to 7 – 10% of a PV cell's available front surface, thus removing metallic contacts to the rear may increase the PV cell efficiency accordingly. The cell structure is demonstrated in Fig.18. N^+ - doped and SiO_2 passivated layers on the front side decrease front surface recombination. N^+ and P^+ parallel narrow no overlapping strips (separated by an efficient electrical insulation) are produced by sequential diffusion processes on the rear of the IBC cell. The rear side surface passivation is provided by covering with SiO_2 layer, through which holes for metallic contacting are made. This way, the cell efficiency over 23% has been reached in mass production. On the other hand, the number of operations increases to 12 or more, which increases the cost of fabrication and resulting cost per W_p is not lower than in the case of standard technology [25].

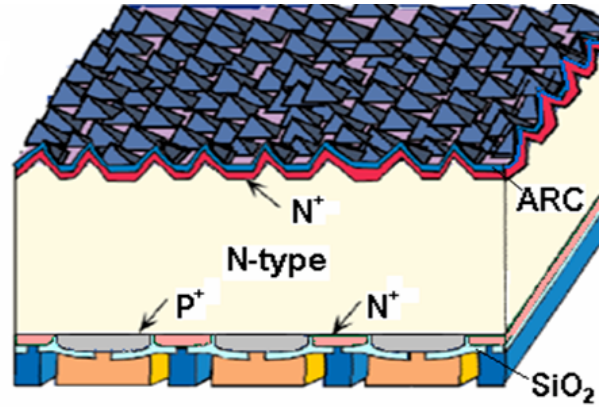

Fig.18. The IBC cell structure

A further increase of efficiency can be obtained using a heterostructure with the top layer from a semiconductor of a wider band gap. In such a structure fabrication are problems, because the lattice constants of all the structure components need to match to give good performance. However, amorphous Si has no well - defined lattice constant and surprisingly appears to perform well as a heterostructure barrier that confines excited carriers to the crystalline silicon and away from ohmic contacts. This is the basic principal of the HIT (heterojunction with intrinsic thin layer) cells. The basic structure is shown in Fig.19. Cells on the base of heterojunction between amorphous and crystalline silicon cells which utilize very thin (10 -20 nm) a-Si:H layer stacks on n-type wafers to provide surface passivation, emitter formation, and a back surface field [26], [27]. The a-Si:H layers are deposited on crystalline silicon by PECVD with very low temperature processes (below 200◦C), avoiding carrier lifetime degradation of the bulk material. On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed. However, the a-Si:H layers cannot be taken to a deposition temperature above 200°C, and this requirement then excludes the use of the standard screen-printed metal pastes and low temperature pastes have 3 times higher resistivity that the standard ones. This requirement for low-temperature metallization can be a significant draw back for HIT cells.

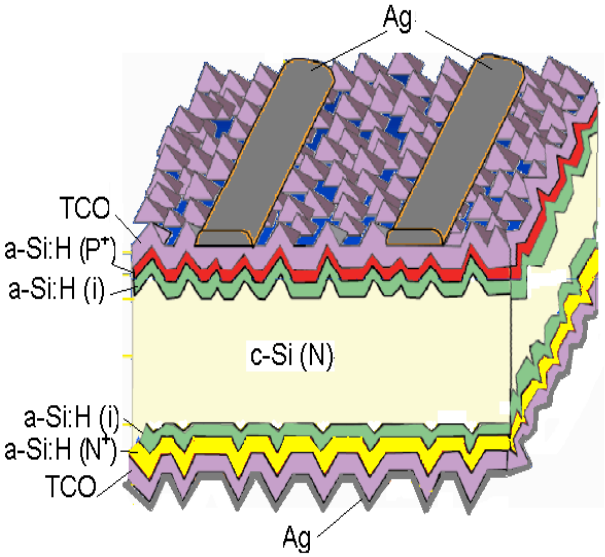

Fig.19. The HIT cell structure

The HIT cells have higher V_{OC} (0.72– 0.73 V), efficiency 22% and offer a lower temperature coefficient (-0.2 to -0.3%/°C) that can be almost half that of a standard c-Si cell [28], which may be very important for applications.

Some further improvements in efficiency may be reached by realization of a tandem structure of a high efficient c-Si cell with a thin film cell [29].

3.2. Module fabrication

Solar cells very similar parameters (sorted at the end of cell fabrication) are used for the module assembly. In standard technology, tinned copper ribbons (tabs) are soldered to the bus bars at the front to connect the back surface of the next cell, as shown in Fig.20 a). The tabs must overlap a long distance along bus bar length since the conductance of the printed bus bars is too low. Tabs provide a no rigid link between cells that allow thermal expansions to be accommodated. The assembly is simplified, if both cathode and anode contacts are on the rear of cells, as indicated in Fig.20 b).

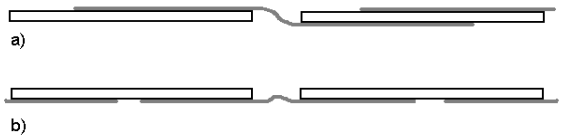

Fig.20. In series connection of two cells using tabs soldered to bus bars

A 2 to 3 mm thick highly transparent soda lime glass (low iron content) is used as a superstrate that provides mechanical rigidity and protection to the module while allowing light through. The cell matrix is sandwiched between two layers of the transparent encapsulant material. The most popular encapsulant is the copolymer ethylene-vinyl-acetate (EVA) with melting point over 95°C, even some other materials can be used [30]. The strings are interconnected with auxiliary tabs to form the cell matrix, which usually consists of several single strings, as shown in Fig.21. Terminals of the strings are brought outside the module to permit flexible circuit configuration.

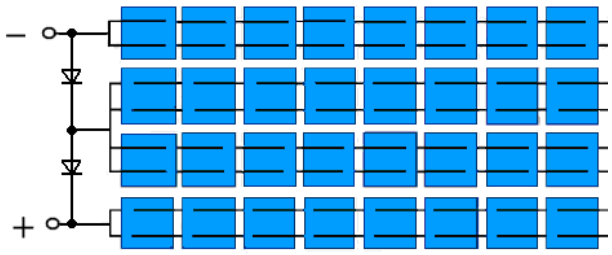

Fig.21. A common c-Si module configuration

The outer layer at the non-illuminated module side is usually a composite plastic (tedlar) sheet or another glass acting as a barrier for humidity and corroding species. The next fabrication steps are lamination and curing [9]. The standard module structure is demonstrated in Fig.22.

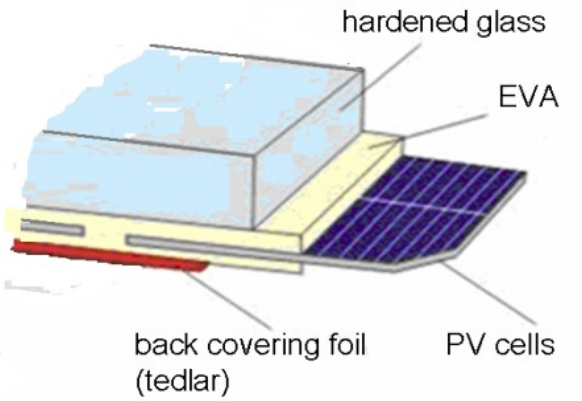

Fig.22. Structure of a standard crystalline silicon PV module

After lamination, the plastic junction box is sticked at the back of the laminate and strings terminals are connected in the junction box. To eliminate possible hot spot origin, the approach followed is to put a diode (bypass diode) in parallel, but in opposite polarity, with a string of cells. Diodes are placed into the junction box.

The most important components of c-Si module fabrication cost are shown in Fig.23. Continuous technological development brings decrease of cost both of silicon and wafering and also some other technological operations.

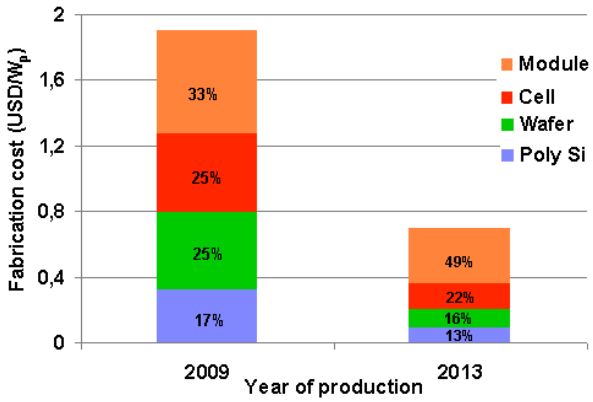

Fig.23. Cost structure of crystalline silicon PV

The module efficiency is lower than cell efficiency due to optical losses by the reflection on the glass – air interface (about 10%). The surface reflection can be lowered by using antireflection coating [31]. The trend is to improve the module power/cell efficiency without significant increasing processing costs.

5. Discussion

Growing demand for photovoltaic applications significantly increased demand for solar grade silicon and after 2005 there was a shortage of starting silicon material. That time were prepared many investments in thin film technologies that start to cover more significant part of the market. From 2008 to 2010, solar-grade silicon production more than tripled [32] from approx. 37,000 MT to approx. 121,000 MT and in 2012 overcame 150,000 MT [33]. This production increase was followed with a considerable decrease of polysilicon cost, as demonstrated in Fig. 24. After resolving the polysilicon bottleneck in 2009, new projects for new wafer based manufacturing sites started to grow significantly, and also the cost of crystalline silicon modules decreased significantly, as shown in Fig. 25. At present, wafer based technology represents approximately 90% of today's market share, whereas all other technologies (including thin film based technologies) represent the remaining 10%. The cost level in 2013 is shown in Fig. 26.

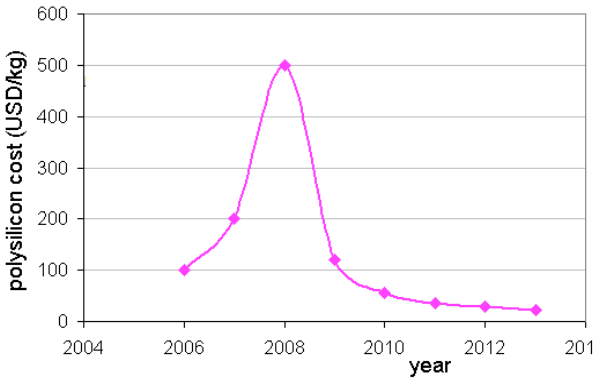

Fig.24. Polysilicon cost development

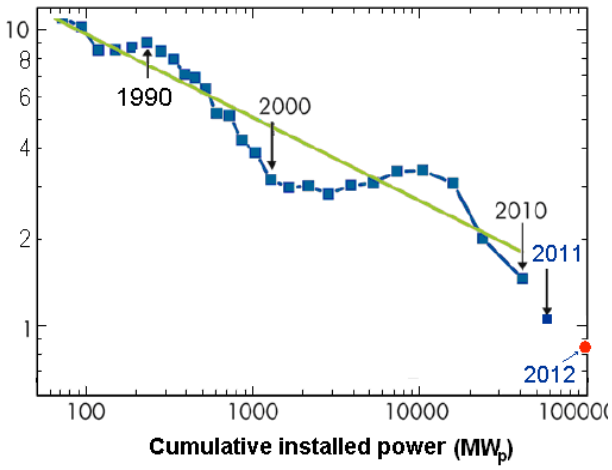

Fig.25. C-Si module price development

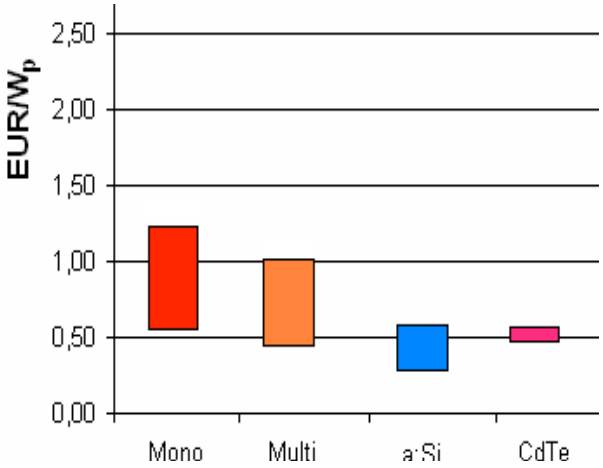

Fig.26. PV module price level in the year 2013

In 2009, the cost of BOS (Balance of System) represented about 40% of the total cost of the system. Since then, the cost of modules has decreased significantly while the cost of BOS slightly increased. The cost of BOS increases with the PV array area, which depend on module efficiency, as indicated on Fig.27. It gives further advantage crystalline silicon modules of higher efficiency that need less BOS portion in the system cost, which is at present higher than 50% [34], as demonstrated in Fig.28. Therefore, the cost of thin film modules should be significantly lower than that of c-Si ones to compete successfully [35]. The development of the market share between crystalline silicon and thin film modules [36] is shown in Fig. 29. The forecasts in PV technologies share in the year 2014 [37] is demonstrated in Fig.30. Both Fig.29 and Fig.30 demonstrate the dominance of crystalline silicon technology at the present market. The most of c-Si modules is fabricated from P-type basic material (84% of total production), but there is a remarkable shift to more advanced cell construction and technologies (selective emitter or MWT technology), which enable fabrication of modules of efficiency up to 17%. There may be also recognised an increase of production of high efficient (>18%) modules fabricated from N-type monocrystalline silicon (IBS or HIT construction). The further increase of the share of the N-type monocrystalline wafer based technologies has been expected [38].

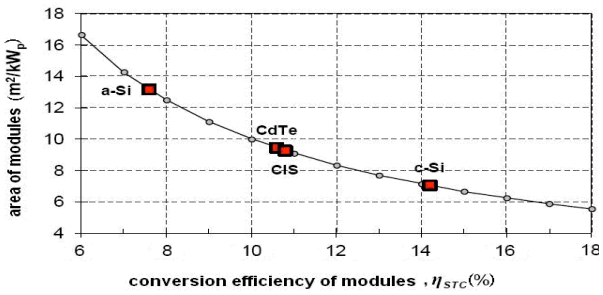

Fig.27. PV array area dependence on module efficiency

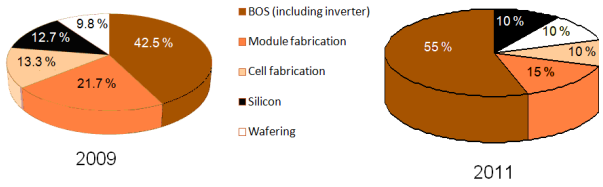

Fig.28. Comparison of the cost structure of PV systems from crystalline silicon modules in 2009 and 2011

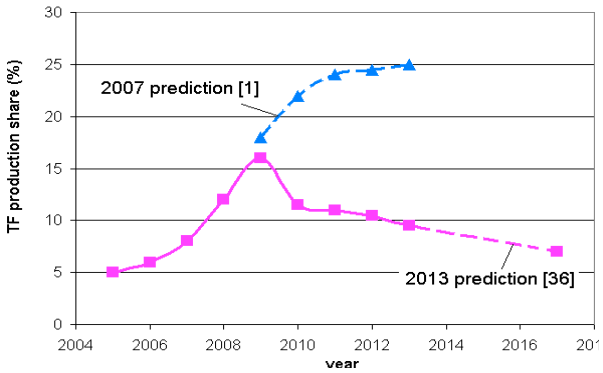

Fig.29. Market share between crystalline silicon and thin film modules development

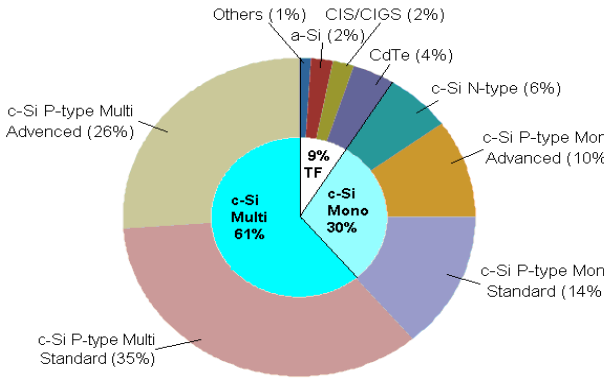

Fig.30. Market share by technology prediction for 2014

From present development follows, that all discussed technologies has reached a module cost level below 1 €/W_p. A roadmap for decreasing cost of crystalline silicon PV modules below 0.5 €/W_p has been discussed in [38].

Very important is also durability of PV modules. At present, durability of minimum 20 years is expected for all technologies on the market, but the efficiency decrease of crystalline silicon modules in PV power stations built in 80's was about 0.5% a year, while the efficiency decrease of thin film module was more than 1% [39]. This gives durability higher than 30 years for crystalline silicon and about 20 years for thin film modules. If typical durability is increased from 20 to 30 years, the cost per generated kWh is reduced by 25%. Therefore, the crystalline silicon will remain the leading technology at minimum for more than following 5 years.

Besides the main technology streams, intensive research and development is done in other very promising new emerging technologies like Dye-sensitised cells, organic cells, quantum dots PV cells and concentrator cells. All these technologies should reach both cost and durability levels of present technologies to find its place on the market.

6. Conclusion

The production processes in the solar industry still have great potential for optimisation both wafer based for the wafer based crystalline silicon technologies that have the role of workhorse of present PV power generation. This is reached by the combination of increased cell and module performance in conjunction with significantly reduced manufacturing cost especially at the cell and module level, by the efficient use of Si and non-Si materials. A decrease of c-Si PV module cost below 0.4 €/W_p before 2015 can be expected. In future, further progress can be achieved by new processes, new tools based on this processes, new materials and new designs of products. Crystalline silicon technologies remain dominant in the field of photovoltaics for more than following five years.

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