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A Review of Nanoscale Channel and Gate Engineered FINFETs for VLSI Mixed Signal Applications Using Zirconium-di-Oxide Dielectrics

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Abstract

In the past, most of the research and development efforts in the area of CMOS and IC's are oriented towards reducing the power and increasing the gain of the circuits. While focusing the attention on low power and high gain in the device, the materials of the device also been taken into consideration. In the present technology, Computationally intensive devices with low power dissipation and high gain are becoming a critical application domain. Several factors have contributed to this paradigm shift. The primary driving factor being the increase in scale of integration, the chip has to accommodate smaller and faster transistors than their predecessors. During the last decade semiconductor technology has been led by conventional scaling. Scaling, has been aimed towards higher speed, lower power and higher density of the semiconductor devices. However, as scaling approached its physical limits, it has become more difficult and challenging for fabrication industry. Therefore, tremendous research has been carried out to investigate the alternatives, and this led to the introduction of new Nano materials and concepts to overcome the difficulties in the device fabrications. In order to reduce the leakage current and parasitic capacitance in devices, gate oxide high-k dielectric materials are explored. Among the different high-k materials available the nano size Zirconium dioxide material is suggested as an alternate gate oxide material for devices due to its thermal stability and small grain size of material. To meet the requirements of ITRS roadmap 2012, the Multi gate devices are considered to be one of the most promising technologies for the future microelectronics industry due to its excellent immunity to short channel effects and high value of On current. The double gate or multi gate devices provide a better scalability option due to its excellent immunity to short-channel effects. Here the different high-k materials are replaced in different Multi Gate MOSFET devices and its performance were studied.

Keywords: Lateral Asymmetric Channel, carrier transport efficiency, System-on-chip (SoC), Equivalent Oxide Thickness (EOT), Threshold voltage roll-off.

1. Motivation to use high k material

In semiconductor industry Moore's Law clearly stated that we will be compressing twice the number of transistors in every 18 months [1]-[3]. The 2012 ITRS(International Technology Roadmap for Semiconductor) update clearly explained that we are progressing towards different high k dielectric materials that will soon replace the gate oxide $Si0_2$ of the devices [4]. As stated in the ITRS (2012 Edition), "The gate dielectric has emerged as one of the most difficult challenges for future device scaling". Indeed, the conventional gate dielectric SiO_2 obviously cannot survive the challenge of an EOT(equivalent oxide thickness) = 1 nm. Also no manufacturable solutions have yet been found to fabricate the SiO_2 thickness, as projected by the ITRS, so it is highly preferable that materials with high dielectric constants and high physical thicknesses will be used for devices [5]. According to Equation. 1, if a dielectric material with a high dielectric constant (high-k) can replace SiO_2 (k = 3.9), the dielectric layer thickness can be increased proportionally while keeping the same capacitance C_{ox}. A figure of merit to judge a high k gate dielectric layer is the EOT, defined as,

$$EOT = (k_{sio2} / k_{high-k}) d_{high-k} \quad [6]$$

The EOT shows the electrical equivalent thickness of the high-k layer to SiO_2 when the capacitance is the same. However, before a new high-k material can be integrated into the present ULSI process flow, many requirements have to be met first [7-10]. One of the most crucial elements that allow the successful scaling in the past is certainly the electrical properties of SiO_2 [7-9]. First, it can be thermally grown on Si with excellent control of thickness and uniformity, which forms a very stable interface on the Si substrate with a low defect density. SiO_2 is thermally stable up to 1000°C, which is required for the MOSFET fabrication. The band gap of SiO_2 is large, i.e., ~9 eV, with sufficiently large conduction and valence band offsets. The dielectric breakdown field is ~ 13 MV/cm. In addition, SiO_2 is water insoluble, which facilitates photolithography. The use of a polysilicon (Poly-Si) gate electrode in the self-aligned CMOS technology was also a determining factor in the scaling. All the key parameters selected gate dielectric materials related to device is listed in Table.1.

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Table 1 List of Key parameters of selected gate dielectric materials. [6, 11, 12]

	Dielectric Constant (k)	Band Gap (Eg, in eV)	Electron Offset (ΦBe, in eV)	Hole Offset (ΦBp, in eV)	Breakdown Field (EBD, in MV/cm)
SiO_2	3.9	9	3.5	4	10
Al_2O_3	8	8.8	3	4.7	10
TiO_2	80	3.5	1.1	1.3	3
ZrO_2	25	5.8	1.4	3.3	4-5
HfO_2	25	6	1.5	3.4	4-5

2. Selection of Zirconium as high k material

There have been many review papers, and industry consensus that proposed a criterion for choosing alternative high-k materials for in MOSFET for different applications. [8, 9, 11, 12,13,14]

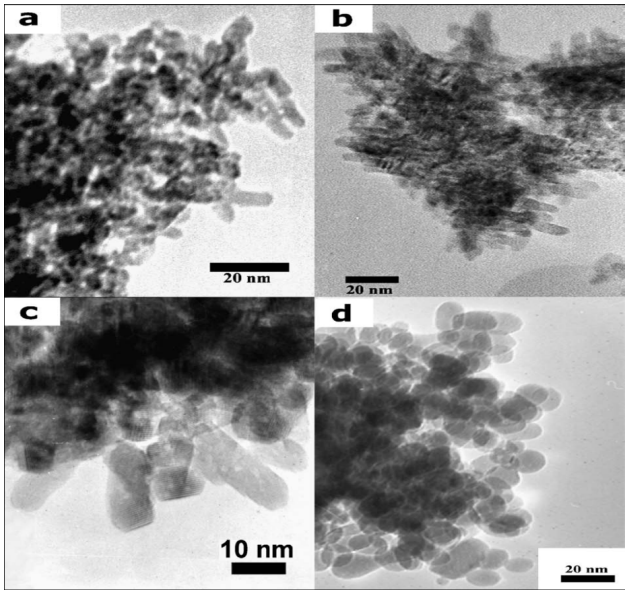

Fig. 1. TEM microphotograph of nanocrystalline ZrO_2 particles prepared by hydrothermal method: a– c—high-temperature hydrolysis of 0.25 M aqueous $ZrO(NO_3)2$ solutions (a—(T = 150 jC, s = 10 min); b—(T = 250 jC, s = 10 min); c—(T = 250 jC, s = 6 h)); (d) hydrothermal treatment of amorphous gel of $ZrO_2.nH_2O$ (T = 250 jC, s = 6 h). [15]

Its observed that Zirconiam-di-oxide is one of the alternate material for gate oxide in the FinFET[75]. Zirconia is the most appropriate metal oxide since it is thermodynamically stable with Si[15].The figure.1 shows the TEM microphotograph of nanocrystalline ZrO_2 particles prepared by hydrothermal method and stability of the material in the nanosize, since it has a dielectric constant value of 25, a large energy bandgap it is suggested for FinFET device. (With values reported from 5.16 to 7.8eV) [16,17].

3. Preparation of Zirconium Dioxide

3.1. Dry chemical process

The wet chemical method is employed for the preparation of ZrO_2 since the powders with different particle size, morphology and phase composition can be prepared by varying parameters such as temperature, duration of the processing, concentration of chemical species to solution.

The zirconia nano particles were obtained by the refinement of zirconium dioxide. The Chemical reactions are as follows[75].

$$ZrO_2 + 4HNO_3 \rightarrow Zr(NO_3)_4 + 2H_2$$

$$2\,Zr(NO_3)_4 + 2\,Na(NO_3) \rightarrow 2\,NaZrO_2 + 5\,N_2 + 13\,O_2$$

$$2\,NaZrO_2 + 2\,HCl \rightarrow 2\,ZrO_2 + 2\,NaCl + H_2$$

The zirconium dioxide (99.9%-AR grade) was purchased from Himedia chemicals. All other chemical reagents in the experiments were of analytical grade and the water used was deionised. Typically the mixed solution of zirconium dioxide (0.04M) and HNO_3 (20ml), with appropriate gram molecular weight, gives the highly hygroscopic zirconium (IV) nitrate salt which is made to be a solution immediately. The solution of Zirconium (IV) nitrate was rapidly mixed with sodium nitrate. The precipitate was filtered and washed with dilute HCl and demonized water repeatedly. Then the precipitate was dried at controlled atmosphere at 100^oC[75]. The outcome of this preparation given the thermally stable with nanosize Zirconium-di-oxide material is observed[75], it gives excellent improvement in the FinFET devices.

4. Limits Of CMOS Technology

Since the 1970s people have been predicting the end of CMOS [18]. Despite these predictions, the monetary benefit of growth has driven massive research, which has overcome all previous barriers [19]. However, many experts are now claiming that the industry is reaching limits that no amount of research can push past. **T**he scaling of CMOS has resulted in a strong improvement in the RF performance of MOS devices [20]. In order to improve device performance, we have to search for a breakthrough in those area involving device structures, material selection, fabrication technology and device operating mechanism to solve problems existing in power, integration density, property optimization and process [21].

There are three key factors limiting continued scaling in CMOS:

- Minimum dimensions that can be fabricated
- Diminishing returns in switching performance
- Off-state leakage

So far the primary limitations to chip scaling have been lithographic issues. In lithographic the research is being done to reduce the minimum wavelength into the extreme ultraviolet spectrum (13 nm wavelengths) [22]. However, transistor dimensions are approaching a physical limit that cannot be overcome. That limit is the size of the atom and molecule of the material. Clearly devices cannot be fabricated smaller than the dimension of a single molecule and some dimensions will need to be more than a molecule wide. It should also be pointed out here that lithographic equipment costs have also grown exponentially [23], and this is beginning to limit the profitability of increased scaling. The dominant non-ideal effect that must be addressed for current scaling to continue is off-state power consumption. Within digital logic, the sources that

contribute to off-state power consumption are: junction leakage, gate induced drain leakage, sub-threshold channel current, and gate tunnel currents. In fact, leakage currents grow exponentially as gate length decreases [24]. To reduce this limits let us move on to the solutions the researchers are proposed.

5. Study of various logic styles and reduce the power:

SILICON-ON-NOTHING

Silicon-On-Nothing transistors with gate length varying from 0.25 um down to 80 nm exhibit excellent performance and scalability. The silicon-on-nothing architecture with thin fully depleted Si film and ultra thin buried oxide results in attenuated short-channel effects , high ON current and high electron mobility[25,28]. The proposed model reproduces the variations of the threshold voltage and sub threshold swing and it is leads for further device optimization.

WAFER BONDING

Wafer bonding is an enabling technology that allows the fabrication of a variety of complicated structures that would be difficult or impossible to make by other means. The process of hydrophobic bonding removes the thin native oxide at surface of silicon wafers. For devices that utilize bulk conduction through the bond interface, this native oxide would reduce or destroy performance by creating traps and electrical discontinuities that will affect the I-V and C-V characteristics at the interface[25,28].

FinFETs

FinFETs have emerged as a superior alternative to replace the conventional bulk MOSFETs to continue the scaling. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped around a thin silicon "fin", which forms the body of the device. The dimensions of the fin determine the effective channel length of the device even down to a 10-nm feature size[25]–[30].

In the literature, FinFET is used generically to describe any fin-based multigate MOSFET architecture regardless of number of gates.

6. Selection Of Finfet

According to the ITRS 2012 [33], MOS transistors will have gate lengths of around 10 nm in 2015.The performance of these transistors is expected to be severely degraded by short-channel effects (SCEs). For sub-100 nm scaling of MOSFETs, double-gate field-effect transistors like FinFETs have attracted considerable attention due to their immunity to Short channel effects and proximity to standard bulk planar CMOS processing [31- 36].

FinFET have been proposed to improve the scalability of the MOSFET, for CMOS technology generations beyond the 22-nm technology node. Since an ultrathin silicon body can effectively suppress SCE, a lightly doped or undoped body can be used in order to achieve high carrier mobilities for improved transistor drive current, as well as to minimize variations in threshold voltage due to statistical doping variations [37]–[38]. So the range of work functions required for thin-body MOSFETs is 4.4 eV–5.0 eV [39], ruling out polycrystalline silicon as a gate material [40].Since the advanced double-gate FinFETs require ultra-thin gate dielectrics for low power consumption. Recently, in FinFET structures with ultra-thin HfO_2 and SiON as gate dielectrics, the gate tunnelling current has been investigated experimentally with the source, drain and substrate electrodes grounded [41],[77]. The reported experimental results provide evidence for reduction of the gate tunnelling current density in narrow FinFET structures compared to their counterpart quasi-planar structures [41].

6.1 Channel and gate engineered FinFETs

FinFET devices shows considerable threshold voltage roll off and DIBL effects. This adverse threshold voltage roll-off effect is the most daunting road block in future MOSFET design. The minimum acceptable channel length is primarily determined by this roll-off [42]-[43],[76]. So here we introduce channel and gate engineering techniques into the FinFETs to reduce subthreshold leakage current and SCE.

In the channel engineering technique, channel is highly doped near the source region to reduce the width of the depletion region in the vicinity of this junction that resulting in reduced subthreshold leakage current and increased output impedance [44]-[45]. This method is called lateral channel engineering, e.g. halo or pocket implants and the engineered channel is known as Lateral Asymmetric Channel (LAC) or Graded channel {GC}. The GC MOSFET is an asymmetric channel device which minimizes the inherent bipolar effects in Fully Depleted transistors [46]. In single halo, an undoped region is preserved in the drain side of the channel. Such undoped region presents negative threshold voltage and can be considered as an extension of the drain region below the gate [47]. Halo implanted devices show excellent output characteristics with low DIBL, higher drive currents, flatter saturation characteristics, and slightly higher breakdown voltages compared to the conventional MOSFET [48]-[49].

In the year 1999 Long et al. [50] proposed a gate engineering technique in which two different materials having different work functions are merged together to form a single gate of a bulk MOSFET. In the DMG structure, the work function of the gate material (M1) close to the source is chosen higher than that close to the drain end (M2) for n-channel FinFETs [51]–[55]. As a result, the electric field and electron velocity along the channel suddenly increase near the interface of the two gate materials, resulting in increased gate transport efficiency, which implies that the threshold voltage under gate material M1 is higher than that under gate material M2. When the drain voltage exceeds the drain saturation voltage, the excess voltage is absorbed by gate metal M2, preventing the drain field from penetrating into the channel. This so-called gate work function engineering allows the DMG devices to have the same threshold voltage for a reduced doping concentration in the channel region, resulting in better immunity to mobility degradation and also higher transconductance [56].

Fig.4 shows the 2D cross-sectional view of a FinFET. In the FinFET, the gate work function is fixed at 4.577eV to obtain the threshold voltage of 0.357 V at a drain voltage of 0.1 V. In Dual Material FinFET,(Fig.4) the work functions of metals M1 (Molybdenum) and M2 (Aluminium) are taken as 4.55 and 4.1 eV, respectively, with equal lengths of L1 and L2, and a threshold voltage of 0.3 V at a drain voltage of 0.1 V is obtained. Optimization of the length and concentration of the halo-doped region for the Single Halo FinFET(Fig.4) was carried out, and the optimum length was found to be 20 nm with a pocket implantation of 7.91×10^{17} cm^{-3}[78]. Increase in the halo doping concentration results in reduced short channel effects but on the other hand results

in increased mobility degradation at the source end and threshold voltage.

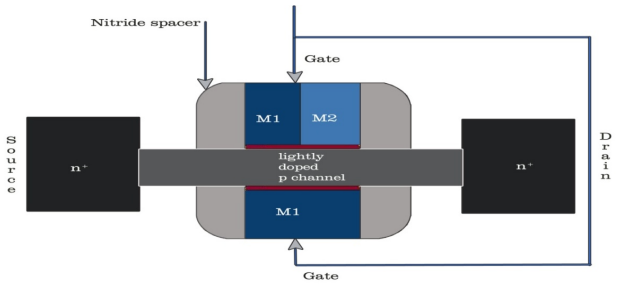

Fig 2. Cross-sectional view of the Dual Material FINFET

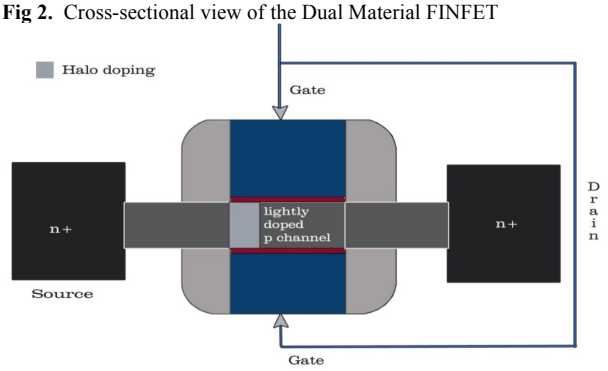

Fig. 3. Cross-sectional view of the Single Halo-FinFET

The leakage current in the channel engineered and gate engineered devices are lesser than the conventional FinFET because of the screening of the drain bias by the step function in the surface potential profile. So any increase in leakage current is suppressed. Gain and output resistance are also higher for these devices. So the Single Halo FinFETs and Dual Material FinFETs can be used for low-power subthreshold analog applications.

7. Novel approach to Dielectrics in FINFET

Since the advent of the metal-oxide semiconductor system over 40 years ago, the SiO_2 gate oxide has been serving as the key enabling material in scaling silicon CMOS technology .With the continuous miniaturization of devices, in order to improve the capability of gate control and control the short channel effect, the gate dielectric thickness should be scaled down with channel length. Facing these challenges, scientists have already proposed some applicable solutions, including new materials, new technologies and device structure innovation. The major advances in Nanosize materials with high-k gate dielectric and metal gate to solve the problems existing in the gate stack and the low power issue [57]-[61]. With the integration of high-k dielectrics into FinFET, the performance of the device is further enhanced. The gate oxide material (SiO_2) in the channel and gate engineered devices are replaced with various high-k dielectrics and the performance of the device is also improved [62]-[63],[79]. The leakage current of the devices are decreased exponentially for high dielectric material which avoids the direct tunnelling of electrons through the insulator. The DIBL which is an important indicator of performance of the devices also decreases exponentially for high dielectric materials thereby suppressing Short Channel Effects of the Nano devices[63]-[64]. The transconductance of the devices also increases with k value. Gain and output resistance of the devices are expected to increase linearly with k value. The most optimized results are can be obtained for devices with ZrO_2 as the gate dielectric. Thus the integration of ZrO_2 nano material dielectrics will improved the performance emerging novel FINFET device .

8. Summary

Most predictions are, if trends continue, CMOS scaling can continue for only a decade or two [65],[66],[67]. There have been many review papers and industry consensus that proposed criteria for choosing alternative high-k materials for different applications [66]-[74]. From the various analysis and investigations of these literatures, Zirconium dioxide was found out to be the best alternative for SiO_2 because of its excellent thermal stability, capacitive performance and insulating properties. So Zirconium dioxide as dielectric nano materials in transistors in the future of nanotechnology . These transistors are expected to show excellent performance and they also show reduce short-channel effects (SCEs). For sub-100 nm scaling of MOSFETs, double-gate field-effect transistors like FinFETs have attracted considerable attention due to their immunity to SCEs and proximity to standard bulk planar CMOS processing. Furthermore the gate and channel engineering techniques employed in FinFETs enhance the device performance to a great extend. These techniques suppress the Short Channel Effects such as DIBL in the FinFETs and also reduces the leakage current. The transconductance and output resistance of the FinFETs increases. The integration of ZrO_2 as gate dielectric in these channel and gate engineered FinFETs further suppresses the leakage current and Short Channel effects making them more applicable for low power subthreshold analog performance.Thus the channel and gate engineered FinFETs with ZrO_2 are promising candidates for the future semiconductor devices for VLSI systems.

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