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Research Article

A Modified High-Efficient Step-Up Sepic for DC Motor Drives

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Abstract

In this paper, Single-Ended Primary Inductor Converter (SEPIC) fed DC motor is proposed. Soft-switching technique such as Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) operation plays a vital role in high voltage applications. Zero-Current-Switching (ZCS) operation achieved due to resonance between the resonant inductor and the capacitor by using output diode and its reverse-recovery loss is subsequently reduced. Zero-Voltage-Switching (ZVS) operation is achieved by using coupled inductor and auxiliary inductor. The model has been simulated through MATLAB/SIMULINK using Diode Bridge, SEPIC topology and closed loop DC motor load and it is modeled analytically. The proposed system is modeled with input side Diode Bridge Rectifier and SEPIC Topology with Proportional Integral (PI) controller. The soft switching scheme for the proposed topology is developed with closed loop motor load. The motor voltage is achieved twice the rated voltage. The results are generated in MATLAB/SIMULINK and are shown.

Keywords: SEPIC topology, voltage multiplier, zero current- switching (ZCS), zero-voltage-switching (ZVS).

1. Introduction

SEPIC converters are mainly used for industrial applications such as power factor correction, photovoltaic system, and LED lighting. Especially in high voltage applications, higher voltage rated power semiconductor devices should be used. When the voltage rating is higher, the Rds (on) of power MOSFETs is higher. So, it causes higher conduction loss at the same level current. Therefore, the overall efficiency can be improved if the voltage stress is reduced with the same decrease in current. To reduce the voltage stress and increase the voltage gain, voltage multiplier techniques are proposed.In order to reduce the volume and weight of the converter, soft-switching techniques such as zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are necessary. However, switching losses and electromagnetic interference noises are significant in high-frequency operation. Therefore, various soft-switching techniques have been introduced. Among them, the active clamp technique is often used to limit the voltage spike effectively, achieve soft-switching operation, and increase the system efficiency. SEPIC converters has low input current ripple but bulk inductor is used in order to minimize the current ripple. It is one of important requirements due to the wide use of low voltage sources such as batteries, super capacitors, and fuel cells. It is because large ripple current may shorten the lifetimes of those input sources.In ZCS PWM SEPIC converter was proposed. Two switches can operate with soft switching. However, three power diodes and three separate inductors are utilized. The voltage stress of the power switches is the sum of the input voltage and the output voltage which is equal to that in the conventional SEPIC converter. In a resonant step up/down converter was proposed. Sort-switching operation is achieved. Two power switches and two magnetic components are required. However, it has a pulsating input current and an additional filter stage is required in the input stage to suppress the input current ripple. Therefore, magnetic components can be increased in number. In, a bidirectional ZVS PWM SEPIC/ZETA converter was proposed. Two main switches can operate with softswitching.

However, a bidirectional switch consisting of two power MOSFETs is required. The voltage stress of the switches in the conventional can be found in proposed SEPIC converter. Parasitic voltage ringing across the bidirectional switches is suppressed by using a snubber circuit.

In conventional SEPIC converter, auxiliary switch and a clamp capacitor are added. The both inductors are utilized to obtain ripple-free input current and achieve ZVS operation of the main and auxiliary switches. The proposed converter achieves high efficiency due to soft-switching characteristics of power semiconductor devices. By utilizing the voltage multiplier technique, voltage stresses of the power switches and diode are reduced by half and the reverse-recovery loss of the output diode is significantly reduced due to the resonance between the resonant inductor and the capacitor in the multiplier circuit.

2. Analysis of the Proposed ZVS Step-Upsepic Converter

The conventional SEPIC converter is shown in Fig. 1. The separate inductor version is shown in Fig. 1(a) and the

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coupled inductor version is shown in Fig. 1(b). In the coupled inductor version, a loosely coupled inductor Lc is used instead of two separate inductors L1 and L2. The Lc has advantages such as single magnetic component and a ripple-free input current. Llk1 and Llk2 are the leakage inductances of the coupled inductor. The magnetizing inductance, the turn ratio, and the leakage inductance Lk2 of the coupled inductor is related with the ripple-free condition. However, the leakage inductance is hard to control in mass production. Fortunately, the leakage inductance Lk1 is not related with the ripple-free condition. Therefore, a tightly coupled inductor can be used with an additional inductor La instead of Lk 2 in Fig. 1(c). The circuit diagram of the proposed soft-switching SEPIC converter with a ripple-free input current is shown in Fig. 2. In the proposed converter, the resonant inductor Lr and the active clamp cell consisting of the auxiliary switch Sa and the clamp capacitor Cc are added to the conventional SEPIC converter shown in Fig. 1(c).Fig. 3 shows the equivalent circuit of the proposed converter. The coupled inductor Lc is modeled as the magnetizing inductance Lm and an ideal transformer with a turn ratio of 1: n. The diodes Da and Dm are the intrinsic body diodes of the auxiliary switch Sa and the main switch Sm. The capacitors Ca and Cm are their parasitic output capacitances. The proposed converter key waveforms are shown in Fig. 4. The duty ratio D is based on the main switch Sm and the switches Sa and Sm are operated asymmetrically. To simplify the steady-state analysis, it is assumed that those capacitors C1, Cc, and Co have large values and the voltage ripples across them can be ignored. Prior to mode 1, the auxiliary switch Sa is conducting. The operation of the proposed converter in one switching period Ts can be divided into five modes as shown in Fig. 5. The magnetizing inductance current iLm is approaching to its minimum value ILm2 and the auxiliary inductor current iLa is approaching to its maximum value ILa1. And the output diode is not conducting.

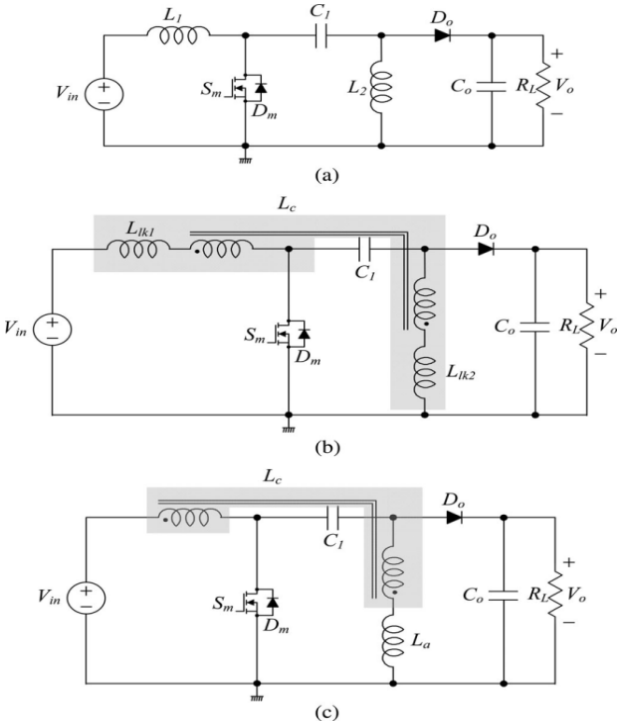

Fig. 1. SEPIC converter (a) Conventional SEPIC converter,Ripple-free SEPIC converter with a (b) loosely coupled inductor, (c)Tightly coupled inductor.

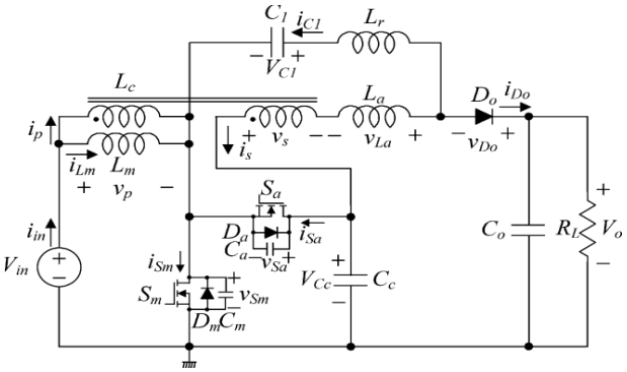

Fig. 2. Proposed ripple-free soft-switching SEPIC.

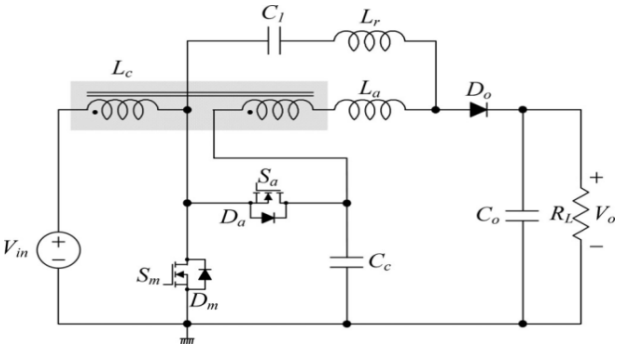

Fig. 3. Equivalent circuit of the proposed converter.

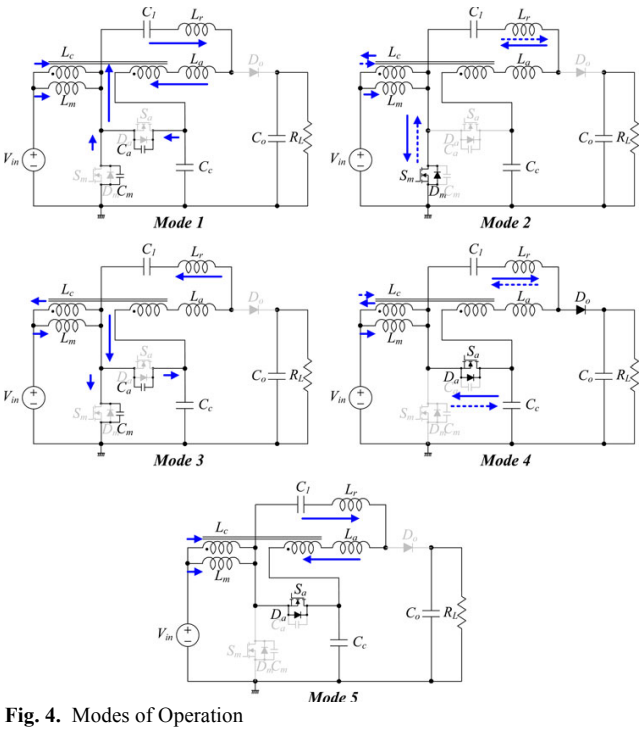

Fig. 4. Modes of Operation

Mode 1 [t0, t1]: At t0, the auxiliary switch Sa is turned OFF. Then, the energy stored in the magnetic components such as Lm, Lr and La starts to charge Ca and discharge Cm. Therefore, the voltage vSa across the auxiliary switch Sa starts to rise from zero and the voltage vSm across the main switch Sm starts to fall from VCc. Since the capacitorsCa

andCm are very small, the transition time interval Tt1 is very short and it can be simplified as follows:

$$T_{t1} = \frac{(C_a+C_m)V_{Cc}}{(1-n)I_{La1}-I_{Lm2}} \quad (1)$$

Since the transition interval Tt 1 is very short, all the currents flowing through the magnetic components are considered constant during this mode.

Mode 2 [t1, t2]: At $t1$, the voltage v_{sm}arrives at zero. Then, the body diode $D_m$is turned ON. After that, the gate signal is applied to the switch $S_m$and the channel of $S_m$takes over the current flowing through D_m. Since the voltage $v_{sm}$is clamped as zero with turn-on of $D_m$before the switch $S_m$is turned ON, zero-voltage turn-on of $S_m$is achieved. In this mode, the input voltage $V_{in}$is applied to$L_m$and the current i_{Lm}increases linearly from its minimum value iLm2as follows:

$$i_{Lm}(t) = I_{Lm2} + \frac{V_{in}}{Lm}(t-t_1) \quad (2)$$

Since the voltage $V_s$at the secondary side of the coupled inductor LcisnV_{in}, the voltage V_{La}acrossLa is$-\frac{V_{Cc}-nV_{in}-V_{C1}}{La+Lr}(t-t_1)$. Therefore, the secondary current$i_s$decreases linearly from its maximum value I_{La1} as follows:

$$i_s(t) = I_{La1} - \frac{V_{Cc}-nV_{in}-V_{C1}}{La+Lr}(t-t_1) \quad (3)$$

The input current $i_{in}$is the sum of $ip$and $i_{Lm}$and given by $i_{in}(t) = i_{Lm}(t) + i_p(t) =$

$$I_{Lm2} + nI_{La1} + \frac{V_{in}}{Lm} + \frac{n(V_{Cc}-nV_{in}-V_{C1})}{La+Lr}(t-t_1) \quad (4)$$

The main switch current i_{sm} in this mode can be derived by

$$i_{sm}(t) = i_{Lm}(t) - (1-n)i_s(t) = -[(1-n)i_{La1} - i_{Lm2}] + \frac{V_{in}}{Lm} + \frac{(1-n)(V_{Cc}-nV_{in}-V_{C1})}{L_a+L_r}(t-t_1) \quad (5)$$

At the end of this mode, the current i_{Lm} arrives at its maximumvalue $i_{Lm1}$and the minimum value i_{La2}.

Mode 3 [t2, t3]: The main switch $S_m$is turned OFF at t_2.Then, the voltage V_{Sm}increases from zero and the voltage V_{Sa}decreases from V_{Cc}at the same time due to the energy stored inthemagnetic components.With the same assumption as inmode1, the transition time interval T_{t2} can be simplified as follows:

$$T_{t2} = \frac{(C_a+C_m)V_{Cc}}{I_{Lm1}-(1-n)I_{la2}} \quad (6)$$

$T_{t2}$is also negligible. All the currents are assumed constantduring T_{t2}.

Mode 4 [t3, t4]: Att_2, the voltage V_{Sa}arrives at zero. Then,the body diode *Da* is turned ON. After that, the gate signal isapplied to the switch $S_a$and the channel of *Sa* takes over thecurrent flowing through D_a.Since the voltage $V_{Sa}$is clampedas zero before the switch $S_a$is turned ON, zero-voltage turnonof $S_a$is achieved.

In this mode, the voltageV_i across $L_m$is-$(V_{Cc}-V_{in})$and the current i_{Lm}decreases linearly from its maximum value i_{Lm1}as follows:

$$i_{Lm}(t) = i_{Lm1} - \frac{V_{Cc}-V_{in}}{L_m}(t-t_3) \quad (7)$$

With the turn-on S_a, the output diode *Do* starts to conduct.Then the resonance occurs between the resonant inductor$L_a$and thecapacitor *C*1. The voltage across the inductor $L_a$is $V_0 + nV_{in} - (1+n)V_{Cc}$, the current increases linearly in thismode as follows:

$$i_s(t) = I_{La2} + \frac{V_0+nV_{in}-(1+n)V_{Cc}}{La}(t-t_3) \quad (8)$$

The input current in this mode is given by

$$i_{in}(t) = I_{Lm1} + nI_{La2} + \frac{V_{Cc}-V_{in}}{Lm} - \frac{n(V_o+nV_{in}-(1+n)V_{Cc})}{La}(t-t3) \quad (9)$$

The current $i_{C1}$is given by

$$i_{C1}(t) = \frac{Vo-V_{C1}-V_{Cc}}{Zr}\sin\omega r(t-t3) - I_{La2}\cos\omega r(t-t3) \quad (10)$$

Where the resonant frequency ω *r*and the impedance *Z* of theresonant tank are

$$\omega_r = \frac{1}{\sqrt{L_r C_1}} \quad (11)$$

$$Z_r = \sqrt{L_r/C1} \quad (12)$$

In this mode, the output diode current $i_{D0}$and the switch currentiS1can be written by

$$i_{D0}(t) = -i_s(t) - i_{C1}(t) \quad (13)$$

$$i_{Sa}(t) = -i_{in}(t) - i_{C1}(t) \quad (14)$$

Mode 5 [t4, t5]: At t_4, the output diode current i_{D0}decreasesto zero and the zero-current turn OFF of the diode*Do* is achieved. Since the current changing rate of *Do* is controlledby a resonant manner, its reverse-recovery problem issignificantly alleviated. The voltage across the inductor$L_a$is $(V_{c1} - nV_{Cc} + nV_{in})L_a/L_a + L_r$, the current *is*increaseslinearly in this mode as follows:

$$I_s(t) = i_s(t_4) + \frac{V_{c1}-nV_{Cc}+nV_{in}}{L_a+L_r}(t-t_4) \quad (15)$$

At the end of this mode, *iLm* arrives at its minimum values ILm2and maximum values ILa1.

3. Design Parameters

A. V_{Cc}ANDV_{C1}

Since the average voltage across *Lm* should be zero under a steady state, the clamp capacitor voltage $V_{Cc}$is obtained by

$$V_{Cc} = \frac{V_{in}}{1-D} \quad (16)$$

Also, the average voltages across the inductors Lrand *La* should be zero. Therefore, the voltage $V_{C1}$is obtained by

$$V_{C1} = V_{Cc} - V_{in} = \frac{D}{1-D} V_{in} \quad (17)$$

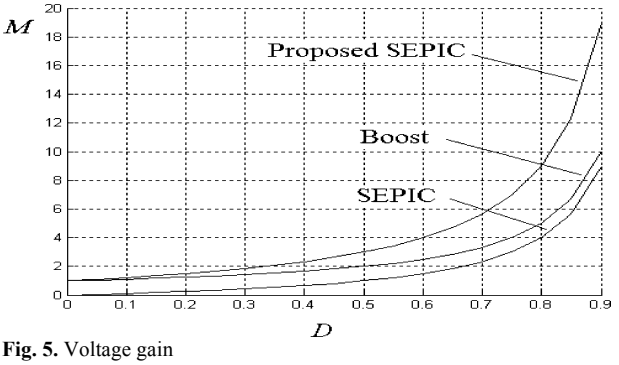

Fig. 5. Voltage gain

B. Voltage Gain

By applying the volt-second balance law to the voltage across the inductor *La* , the following relation is obtained:

$$-\frac{L_a}{L_a+L_r}(V_{Cc} - nV_{in} - V_{C1})DT_s + \frac{L_a}{L_a+L_r}(V_{C1} - n(V_{Cc} - V_{in}))(1 - D - d_2)T_s = 0 \quad (18)$$

From (16) to (18), the proposed converter voltage gain *M* can be obtained by

$$M = \frac{V_o}{V_{in}} = \frac{1}{1-D}\left[1 + nD + \frac{(1-n)DL_a}{L_a+L_r}\right] \approx \frac{1+D}{1-D} \quad (19)$$

The voltage gain of (19) is plotted and compared with other converters in Fig. 6.

C. Input Current Ripple

In mode 2, the input current *i*in is given by (4). From (16) and (17), the ripple component of *I*in can be removed by satisfying the following condition:

$$L_a + L_r = n(1-n)L_m \quad (20)$$

Under the condition of (20), the input current $i_{in}$is constant as $I_{Lm2} + nI_{La1}$. In mode 4, the input current $i_{in}$is given by (9).Similarly, from (16), (17), and (19), its ripple component can be removed by satisfying the same condition of (20). In this mode, the input current $i_{in}$is constant as $I_{Lm2} + nI_{La1}$. From (19), it can be seen that the inductor current iLahas the same slope both in mode 4 and 5. Therefore, the input currenti_{in}does not change in mode 5. From (2), $I_{Lm1} - I_{Lm2}$ is obtained by

$$I_{Lm1} - I_{Lm2} = \frac{V_{in}}{L_m} DT_s \quad (21)$$

Similarly, $I_{La1} - I_{La2}$ is obtained from (3) as follows:

$$I_{La1} - I_{La2} = \frac{V_{Cc} - nV_{in} - V_{c1}}{L_a+L_r} DT_s \quad (22)$$

With the condition of (20), the following relation can be easily derived from (16), (17), (21), and (22):

$$I_{Lm2} + nI_{La1} = I_{Lm1} + nI_{La2} \quad (23)$$

Therefore, the ripple component of the input current i_{in} can be removed under the condition of (20).

D. Minimum and Maximum Values of Ilm and Ism

From Figure3$i_s = i_{C1} + i_{Do}$. Since the average capacitorcurrent i_{C1avg} should be zero under a steady state, the average valueof the capacitor current $i_{C1}$is zero. And the average outputdiode current $i_{Doavg}$is equal to the average output current I_o. Therefore, the following relation can be obtained from thewaveform of the secondary current $I_s$in Figure 4

$$I_{La1} + I_{La2} = -2I_o \quad (24)$$

From (16), (17), (20), (22), and (24), the maximum and minimumvalues of $I_s$are derived by

$$I_{La1} = \frac{(1-n)V_{in}DT_s}{2(L_a+L_r)} - I_o \quad (25)$$

$$I_{La2} = \frac{-(1-n)V_{in}DT_s}{2(L_a+L_r)} - I_o \quad (26)$$

Similarly, from Fig. 3, the input current $i_{in}$is the sum of $i_p$and i_{Lm}. Since the average current $i_{savg}$is $-I_o$, the average primarycurrent $i_{p,avg}$is equal to $-nI_o$. Therefore, the following relationcan be obtainedfrom the waveform of the magnetizing currenti_{Lm}in Fig. 4:

$$I_{Lm1} + I_{Lm2} = \frac{2P_o}{\eta V_{in}} + nI_o \quad (27)$$

where η is the efficiency and *Po* is the output power. From (21) and (27), the maximum and minimum values of I_{Lm} are derived by

$$I_{Lm1} = \frac{P_o}{\eta V_{in}} + nI_o + \frac{V_{in}DT_s}{2Lm} \quad (28)$$

$$I_{Lm2} = \frac{P_o}{\eta V_{in}} + nI_o - \frac{V_{in}DT_s}{2L_m} \quad (29)$$

E. ZVS Condition

From Fig. 4, the ZVS condition for $S_a$is given by

$$I_{Lm1} - (1-n)I_{La2} > 0 \quad (30)$$

SinceI_{Lm1} is always positive from (28) and $I_{La2}$is alwaysnegative from (26) for *n* <1, the condition of (30) is alwayssatisfied for *n* <1. Therefore, the ZVS of $S_a$is always achieved.Similarly, for the ZVS ofS_m, the following condition should besatisfied

$$-I_{Lm2} + (1-n)I_{La1} > 0 \quad (31)$$

From (19), (25), and (29), the inequality (31) is rewritten by

$$L_m < \frac{V_{in}DT_s}{2n(M/\eta+1)I_o} \quad (32)$$

F. ZCS Condition

From (8), (10), and (13), the output diode current reset timingratio d2 can be obtained by solving the following equation:

$$-I_{La2} - \frac{V_o + nV_{in} - (1+n)V_{Cc}}{L_a} d_2T_s - \frac{V_o - V_c - V_{Cc}}{Z_r}\sin\omega_r d_2T_s + I_{La2}\cos\omega_r d_2T_s = 0 \quad (33)$$

To obtain ZCS of the output diode, the following conditionshould be satisfied

$$d_2 < 1 - D \quad (34)$$

G. Voltage Stresses of the Power Switches and Output Diode

From Figure 2, it can be seen that the voltages across the mainand auxiliary switches are confined to the clamp capacitor voltageV_{Cc}. By using (16) and (19), the voltage V_{Cc}can be rewrittenas $(V_{in}+V_o)/2$. Since the voltage stress of the power semiconductordevices in the conventional SEPIC converters shown inFigure 1 is $V_{in}+V_o$, the voltage stress in the proposed converteris reduced by half. In the proposed converter, the voltage stressof the output diode is also reduced by half. In mode 2, thevoltage $V_{La}$is $-(V_{Cc} - nV_{in} - V_{c1})L_a/L_a + L_r$.Therefore, themaximum voltage $V_{Do,max}$across the output diode is given by

$$V_{Do,max} = V_o + \frac{(1-n)V_{in}L_a}{L_a+L_r} + nV_{in} - V_{Cc} \quad (35)$$

For $L_a \gg L_r$, it can be easily seen that $V_{Do,max}$is $(V_{in} + V_o)/2$,which is half of that in the conventional SEPIC converters.

4. Simulation Circuits

A prototype of the classical boost is also built with the same specification of the proposed converter. The circuit is shown in figure 6.

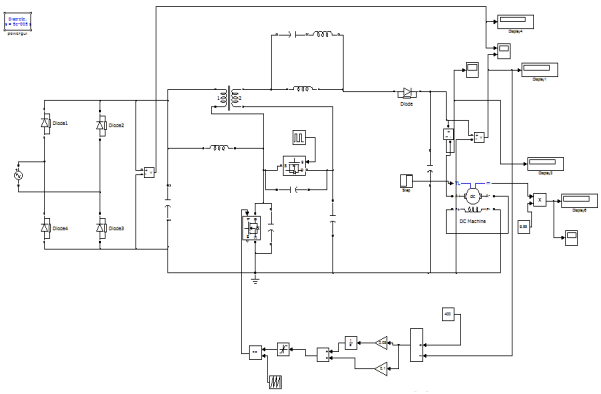

Fig. 6. Proposed Simulation Circuit

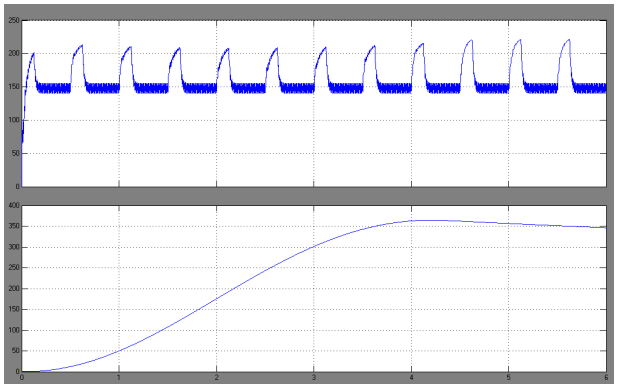

Fig 7. Input voltage (Vi) and output voltage (Vo) waveform for an input voltage Vi= 230Vrms

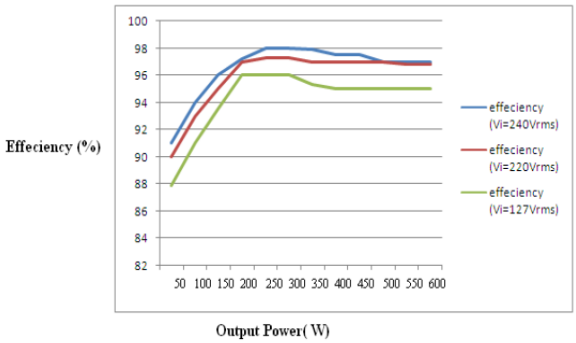

Fig. 8. Efficiency curves of the proposed converter as a function of the output power.

The output power is reduced from the nominal value Po= 650 W to Po= 300 W, and the output voltage rises from the nominal value Vo= 425 V to the maximum value Vo= 465 V during the load transient. The transient duration is also 150 ms. Therefore, the overshoot of the output voltage presented by the proposed converter is equal to 11.76%, and the overshoot of the classical boost converter is equal to 9.4% for the same controller parameters. Figure 7 presents the output voltage (Vo) and input inductor current (iLboost) of the boost converter Output voltage (Vo) and input inductor current (iLboost) of the boost converter operating with Vi= 127 Vrms and with the output power reduction from 650 to 300 W.

5. Experimental Results

To verify the steady-state performance and the theoretical analysis of the proposed soft-switching SEPIC converter with ripple-free input current, a laboratory prototype is implemented and tested with the following specification.

1) Input voltage *Vin* = 10V.
2) Output voltage *Vo* = 20V.

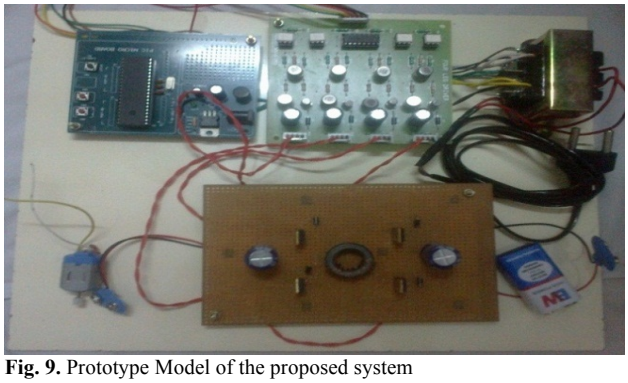

Fig. 9. Prototype Model of the proposed system

The control circuit was implemented with a constant frequencypulse width modulation controller KA7552 from Fairchild. The required voltage gain *M* is 4.17. From (19), the duty cycle *D* is calculated as 0.613. The turn ratio *n* of the coupled inductor is selected as 0.25. The magnetizing inductance *Lm* is selected as 190 μH. Then, the condition for ripple-free input current of (20) gives *La* + *Lr* = 35.6 μH. Then, the values of the inductors *La* and *Lr* are selected as 34.5 and 1.1 μH, respectively. The value of *Cr* is selected as 1 μF to meet the condition of (34). The values of the capacitors *Cc* and *Co* are selected as 6.6 and 100 μF, respectively. Figure 7 shows the experimental waveforms of

*i*in,*is* , and *vSm* under various load conditions. Regardless of load condition, the proposed converter shows almost ripple-free input current. In Figure 7, the main switch voltage *vSm* is well clamped as around 124V, which agrees with the theoretical analysis.

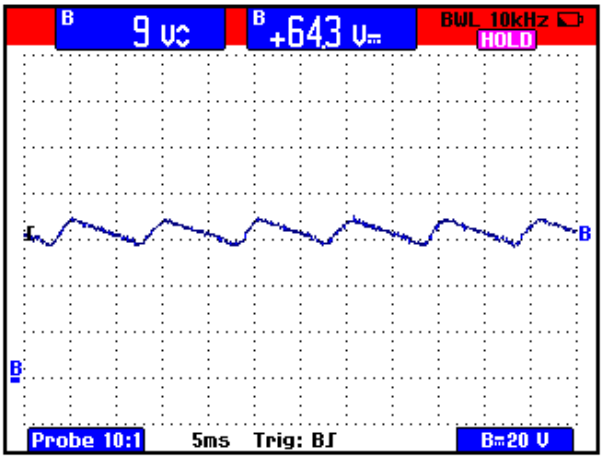

Fig. 10. Hardware result of Output voltage

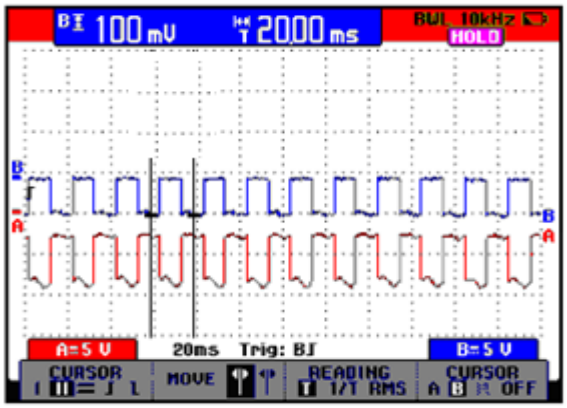

Fig. 11. Hardware result of Thyristor firing pulse

It can be seen that the resonance between *Lr* and *C*1 occurs and the resonant current flows through the output diode during turn-off of *Sm*. The experimental results are in good agreement with the theoretical analysis. The resonance between *C*1 and *Lr* ends before the turn-on of *Sm*. Since the voltage *vDo*is maintained as zero after the current *iDo* arrives at zero, the turn-off loss of the output diode is seen to be almost zero and the ZCS operation of *Do* is achieved. Also, thereverse recovery of the output diode is significantly alleviated.It is observed that the gate pulses are driving the main switch *Sm*, only after the switch voltage *vSm* has reached zero. It indicates the zero voltage turn-on of *Sm*. Similarly, the auxiliary switch *Sa* is turned ON at zero voltage as shown in Figure 9. Figure 12 shows the measured efficiency of the proposed converter and it is compared with that of the conventional SEPIC converter in Figure 1(a).The proposed converter exhibits an efficiency of 94.8% at full load condition. The proposed converter shows higher efficiency than the conventional SEPIC converter due to its soft-switching characteristic of power switches *Sm* and *Sa* and the output diode *Do*. At light load, the proposed converter shows lower efficiency. It is mainly because the secondary current *is* increases the conduction loss and it makes up a significant portion of the power loss at light load. As shown in Figure 7, the current *is* is large even at light load. It is one of the major drawbacks of the proposed converter.

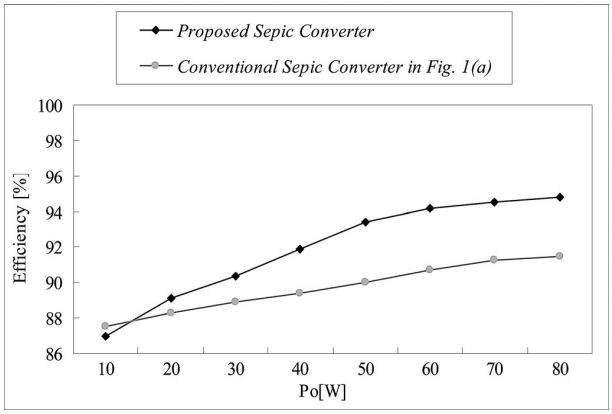

Fig. 10. Measured efficiency.

6. Conclusion

The operation principle, theoretical analysis, and the implementation of a soft-switching SEPIC converter with ripple-free input current are presented in this paper. In the proposed converter, the coupled inductor with an auxiliary inductor is used to provide ripple-free input current and achieve ZVS operationof main and auxiliary switches. The advantages of the proposed converter are low voltage stresses, low switching losses, ripplefree input current, alleviated reverse-recovery problem of the output diode, and high efficiency. The design consideration of the proposed converter is included. The experimental results based on a prototype are presented for validation.

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