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A Novel Gan Hemt Cascode Microwave Power Amplifier for Wireless Communications

Hoang Anh Dang[1], Van Dung Tran[2], Duy Manh Luong[3], Xuan Loi Dai[4], Phuong Nhung Do[1], Nghia Hoang Trong[1], Nguyen Thi Phi Doan[1] and Long Tran Huy[5]

[1]*Faculty of Electrical and Electronic Engineering, Hanoi Open University (HOU), B101 Nguyen Hien, Hai Ba Trung, Hanoi, Vietnam*
[2]*Institute for Technology Development Media and Community Assistance (IMC), 176 Truong Chinh, Dong Da, Hanoi, Vietnam*
[3]*Dept. of Radio-Electronic Engineering, Le Quy Don Technical University, 236 Hoang Quoc Viet, Cau Giay, Hanoi, Vietnam*
[4]*Military Institute of Science and Technology, 100000 Hanoi, Vietnam*
[5]*Posts and Telecommunications Institute of Technology, Hanoi, Vietnam*

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Abstract

A novel cascode-type GaN HEMT circuit is proposed in the present study. The independent bias method is used to improve linearity as well as efficiency. At one tone operation, the proposed power amplifier of 2.1-GHz has a power gain of 16.5 dB, and 32 dBm output power with an efficiency of 66%. In addition, the proposed amplifier achieves an efficiency of 35.8% and 19.7-dB power gain with a IMD3 level of -35 dBc, for a 4-MHz spacing two-tone operation. The proposed amplifier is compared with a conventional amplifier. It shows that the proposed amplifier offers superior performance over the conventional one in terms of efficiency as well as linearity.

Keywords: Cascode amplifier, GaN HEMT, wireless communications, adaptive control, SSPA, IMD3

1. Introduction

Microwave power amplifier (PA) plays a crucial role in modern wireless communication systems including cellular networks, PAR (phased array radar), broadcasting systems, and electronic warfare [1-2]. The operation of the PAs can be categorized into two main types: linear mode and peak mode. For the latter (peak) mode, they are optimized for best efficiency. In the other (linear) mode, the focus shifts towards achieving the highest possible linearity performance [3]. Extensive evidence supports the notion that PAs cannot effectively deliver high efficiency and linearity concurrently. In the fact that simultaneously balancing high efficiency and high linearity in PAs is challenging [4]. Novel designs like a stacked Ku-band PA with 2 output channels have shown promising electrical properties such as high output power, wide bandwidth, and excellent power stability. By optimizing parameters like bias voltage and input RF power, PAs can minimize DC power consumption while meeting received SNR constraints, enabling the evaluation of highly nonlinear classes for satellite communication applications. Different techniques and solutions have been proposed to enhance the PAs' efficiency while maintaining linearity. Popular classes of operation like D, E, F, and F^{-1}, as well as harmonic tuning approaches, can boost efficiency but often result in degraded linearity due to low conduction angles [1]. To address this, linear PAs have been introduced, including feedforward PA, pre-distortion PA, and Doherty PA, each employing unique methods to improve linearity performance [5-6]. For instance, the Doherty power amplifier (DPA) utilizes an auto-tuning process and digital pre-distortion to optimize configuration and linearize the amplifier, achieving improved linearity with high efficiency. Additionally, the CMOS quadrature power amplifier (QPA) technique enhances linearity, bandwidth, efficiency, and power consumption by separately amplifying amplitude and phase quadrature signals, showcasing advancements in linear SSPA design [7].

A specialized method is implemented in this category of PAs to enhance the linearity performance [17-22]. While PAs employing the feedforward technique can attain exceptional linearity performance, their structure is intricate due to integrating numerous individual components. An alternative linearization method is utilized to simplify the circuit architecture, such as pre-distortion in analog and digital formats. Another prevalent and promising approach for developing linear PAs is the utilization of a DPA. This amplifier type comprises two constituent amplifiers - the carrier and the peaking amplifier. The latter mentioned amplifier operates with biasing in class B or class AB, and the carrier amplifier is biased in class C. By employing a specific methodology, the PA efficiency can be enhanced when the output power is reduced from saturation levels. Despite possessing remarkable linearity, the efficiency of these linear PAs experiences a degradation.

From the above considerations, the goal of this study is proposing a novel circuit for the linearity and efficiency improvement of the SSPAs while simultaneously surmounting the drawbacks of traditional design methods. It is widely known that a conventional cascode-type circuit can deliver various promising advantages including high gain, high isolation and wide bandwidth [23-24]. However, one main drawback of such a circuit is its stacked point between the two transistors. This causes a degradation of important circuit performances, including efficiency and linearity. This

*E-mail address: anhdh.dttt@hou.edu.vn
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is because the operation condition of each transistor becomes inter-independent. The proposed circuit is implemented by adding a bias line to the common point between two transistors. Therefore, the bias condition can be controlled independently for each transistor. It has been proved that by applying such a method to a bipolar junction transistor (BJT)-type cascode configuration, efficiency, and linearity can be significantly improved [25-26]. In the present study, we employ a similar technique for the field effect transistor (FET)-type cascode configuration. The essential advantage of the proposed circuit is the ability to simultaneously improve linearity as well as efficiency. In particular, demonstrations of linearity in terms of ACPR, which is really important in modern wireless communication systems, and bandwidth in terms of efficiency bandwidth of the proposed circuit are presented in the present study.

The remaining sections of the paper are structured as follows. Section 2 provides a comprehensive overview of the proposed circuit. An analysis the efficiency and linearity of this configuration is carried out in Section 3. Section 4 presents a step-by-step design methodology for an PA utilizing the proposed circuit configuration. Furthermore, the performance of the designed PA is assessed and compared to that of a traditional PA in the same section. Lastly, Section 5 serves as the conclusion of the paper.

2.Background

2.1 Independent Bias

Fig. 1 illustrates the a conventional cascode circuit and an independent bias cascode circuit. Here, it is noted that the proposed circuit is able to adjust the operation condition for every transistor, while it is impossible for the conventional one. A biasing scenario for these circuits is illustrated in Fig. 2 to demonstrate the advantages of such a proposed technique.

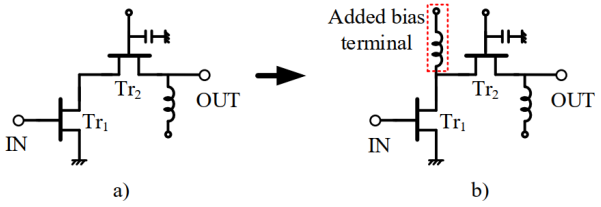

Fig. 1. Circuit topology: a) Conventional; b) Independent bias

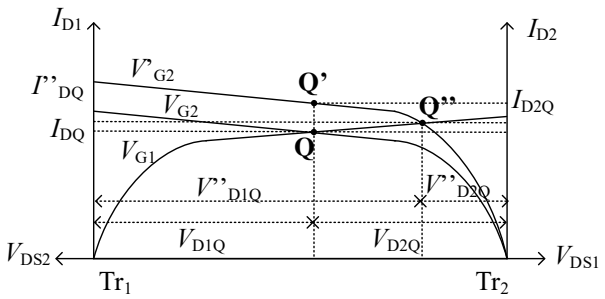

Fig. 2. Biasing for the conventional and proposed circuits

As shown in Fig. 1a, two requirements must be fulfilled for the conventional circuit. The first one is the total drain bias voltage ($V_D = V_{D1Q} + V_{D2Q}$), which has to be unchanged regardless of the bias point. The second one is the drain currents flowing through two transistors with the same magnitude and direction. This means if the initial bias point Q moves to another point Q', which has a higher gate bias voltage for the second transistor ($V'_{G2} > V_{G2}$), it will be pulled down to a bias point Q" to keep equal drain currents through Tr1 and Tr2 ($I"_{D.Q.}$) and to keep equal total drain voltage ($V_{.D.}$). This behavior implies that the operation condition cannot be controlled independently for each transistor due to the stacked point, as mentioned. On the other hand, if an additional bias terminal is added at the common point between Tr1 and Tr2, the bias point Q can move freely to Q' since, in this case, the drain current of each transistor is not necessarily to have the same magnitude and direction. Moreover, the operation of each transistor can be adjusted independently. The advantage of setting independently biased conditions is that it helps to improve the linearity as well as efficiency of the SSPA simultaneously. In the following section, the performance of such a proposed circuit will be investigated depending on the variation of bias conditions.

2.2 Performance Evaluation for two configurations

This section evaluates the critical performance of the proposed amplifier, including PAE (power added efficiency) and linearity in terms of third-order intermodulation distortion (IMD3), under various bias conditions at 2.1 GHz. The circuit diagram of the investigated amplifier is indicated in Fig. 3. It comprises the proposed cascode circuit. Its performance is evaluated using a Harmonic Balance analysis embedded in the Keysight ADS simulator.

Here Z_{Sopt} denotes the optimum source and Z_{Lopt} denotes the load impedances obtained using the load/source pull simulation technique. The independently biased technique helps to make adaptive control of bias terminals, including V_{g1} and V_{d1} and V_{g2} and V_{d2}.

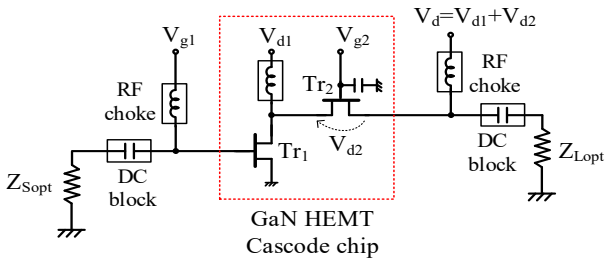

Fig. 3. Circuit schematic for investigation of performance

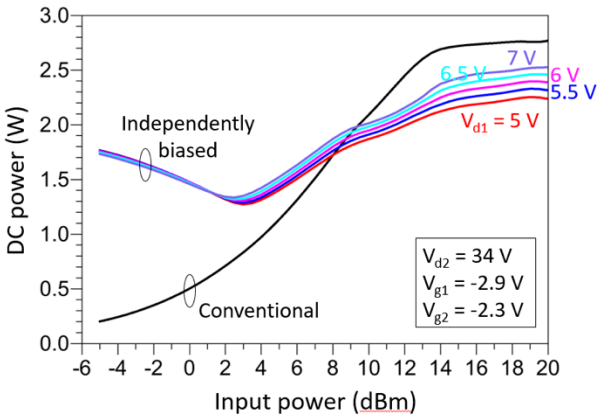

Fig. 4. D.C. power of two cascode configurations

a. Efficiency Validation

The circuit's efficiency relies on bias terminal Vd1, affecting D.C. power usage. Proper Vd1 control reduces D.C. power supply, increasing efficiency. Fig. 4 shows D.C. power comparison between different bias configurations.

Conventional configuration has lower D.C. power at low input power. Adjusting Vd1 boosts efficiency at high input power levels, shown in Fig. 5.

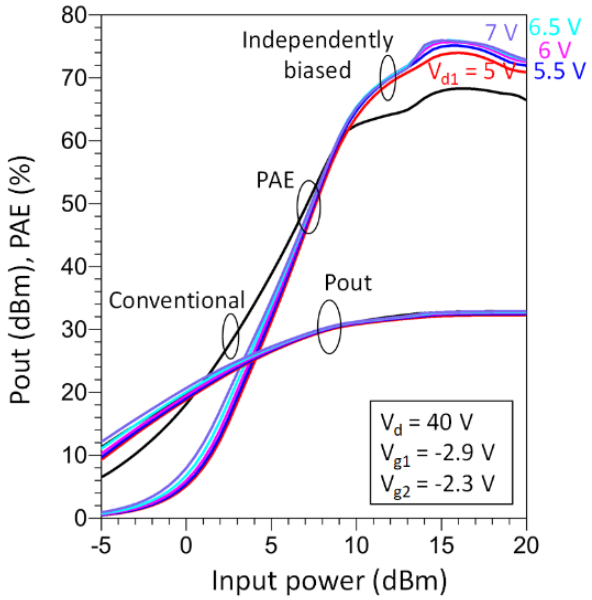

Fig. 5. Comparison of simulated output power and efficiency

Fig. 5 shows that the PAE of the independently biased cascode configuration can be enhanced because of the reduced D.C. power, as expected. Here it is worth noting that the bias conditions of the two configurations are similar for a fair comparison. This means the total drain bias voltage V_d and gate bias voltages V_{g1} and V_{g2} are identical for both configurations.

b. Linearity Validation

The linearity of the proposed circuit relies heavily on the added bias terminal, which aids in internal nonlinear compensation between transistors. This phenomenon is visually depicted in Fig. 6. Two signals of equal power and 4 MHz frequency spacing are fed into the circuit during simulation. Varying Vd1 affects the IMD3 of the proposed circuit, enhancing it compared to the conventional circuit.

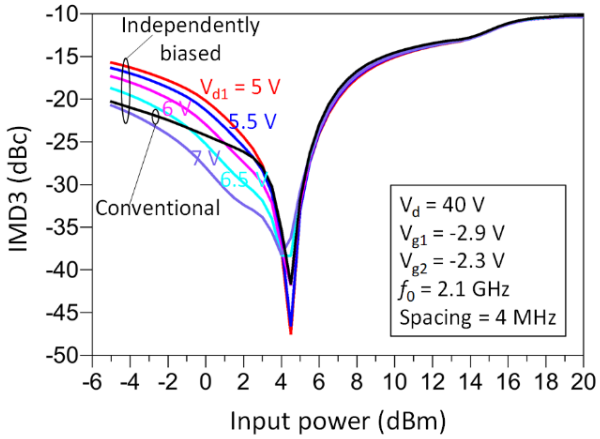

Fig. 6. Simulated IMD3 investigation depending on the change in Vd1

3. The proposed GaN HEMT Cascode performances

A microwave power amplifier employing the proposed structure is designed and simulated to demonstrate the advantages of such a proposed cascode circuit configuration that have been investigated. Its performance is also compared with that of the conventional cascode amplifier.

3.1. General Consideration

A GaN HEMT device with a 75-µm gate width and 4 fingers is used in the design phase. The study primarily aims to design a microwave power amplifier to improve its efficiency and linearity simultaneously, owing to the independently biased technique. From the previous investigations carried out in Sec. 3, the bias condition for each transistor is optimized for both efficiency and linearity as follows. The first common-source HEMT of the proposed circuit is operated around class-B (V_{DS} = 6 V, V_{GS} = -2.9 V) to obtain high-efficiency, and the second common-gate HEMT is operated near class AB (V_{DS} = 34 V, V_{GS} = -2.5 V) for the improvement of the linearity as described in Fig. 7. For high-efficiency design purpose, harmonic termination method will be employed in this study. This method is explained as follow:

$$v_{DS}(t) = V_0 + \sum_{n=1} \sqrt{2} V_n \sin(n\omega_0 t + \phi_n) \quad (1)$$

$$i_{DS}(t) = I_0 + \sum_{n=1} \sqrt{2} I_n \sin(n\omega_0 t + \phi_n + \theta_n) \quad (2)$$

where $v_{DS}(t)$ is voltage and $i_{DS}(t)$ is current at the output of the active device; V_0 and I_0 are DC components of the output voltage and current, ω is the operation angular frequency while ϕ_n and θ_n are phase components. The dissipated power inside the transistor is given as following:

$$P_a = \frac{1}{T}\int_0^T v_{DS}(t) i_{DS}(t) dt = V_0 I_0 + \sum_{n=1} V_n I_n \cos\phi_n \quad (3)$$

Hence, to reduce the power dissipation or improve the efficiency, both the two following requiments must be satisfied:

$$V_0 I_0 + V_1 I_1 \cos\phi_1 = 0 \quad (4)$$

$$\sum_{n=2} V_n I_n \cos\phi_n = 0 \quad (5)$$

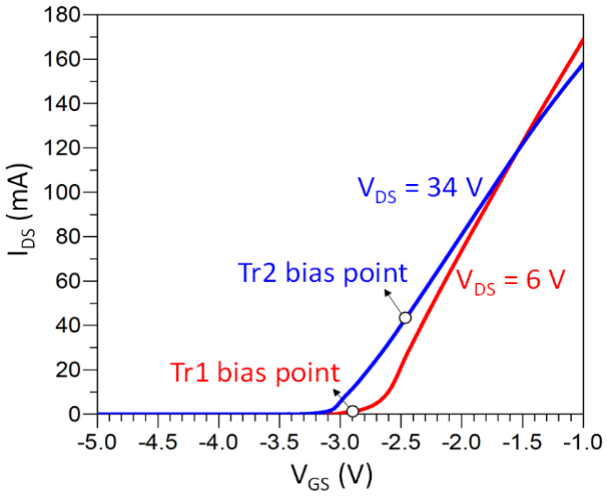

Fig 7. Bias condition for each transistor of the proposed cascode configuration

Formular (4) implies that the DC power will be transformed to the output power at the fundamental frequency. Condition (5) means that harmonic power is dissipated. These conditions are realized by using a load/source pull simulation in the Keysight ADS. By utilizing this technique, the source/load impedances at the fundamental frequency and second harmonic that satisfy (4) and (5) are shown in Fig. 8.

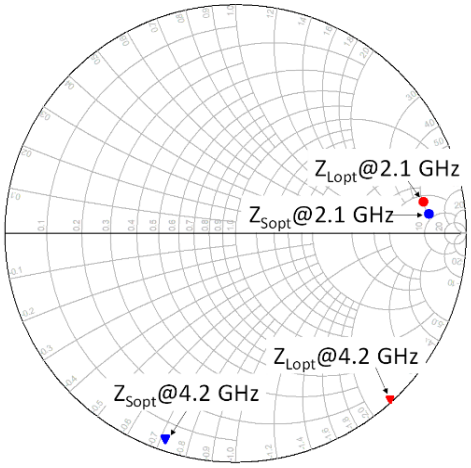

Fig. 8. Simulated optimum load and source impedances realized using the load/source pull technique

3.2. Bias Network Design

It can be seen in Fig. 8 that the impedances at second harmonic are located close to edge of the Smith chart that means a pure reactance. This implies the phase difference between current and output voltage at the second harmonic is ±π/2 or condition (5) is satisfied. In addition, expression (4) is fulfilled with the optimum load and source impedances at 2.1 GHz. After that, the matching circuits and biasing circuits will be designed. In this paper, the matching and biasing circuits are implemented on microstrip technology using a substrate with the following parameters: 0.75-mm substrate thickness; 0.35-um conductor thickness; dielectric constant of 3.7; dielectric loss tangent of 0.002.

A biasing circuit is designed first, and then the input/output matching circuits is designed. The main function of the biasing circuit is providing DC power to the PA and isolating the RF signal at the fundamental frequency. Moreover, the linewidth of the bias line is reduced in order to realize high impedance condition. Fig. 9 shows the frequency response simulation of the designed bias circuit. The results indicate a low loss behavior at 2.1 GHz with S_{21} of -0.04 dB and S_{11} of -35 dB.

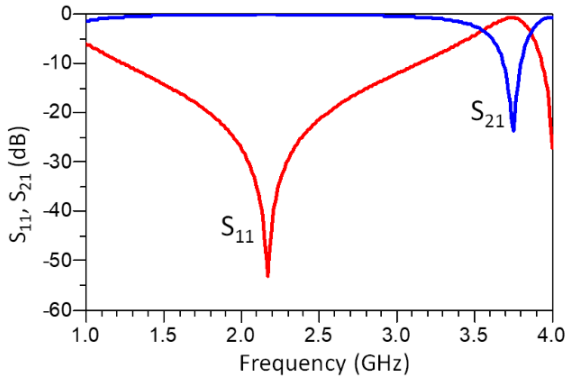

Fig. 9. Frequency response of the designed bias circuit

3.3. Input/Output Matching Network Design

This section presents the design of low-loss matching circuits for impedances at the fundamental frequency and the second harmonic frequencies. The design strategy is explained. Use open stub as the quarter-wave line at 4.2 GHz for reactive impedance. Tune transmission lines for optimum impedance at 2.1 GHz. EM models in Fig. 12 show output and input matching networks with bias networks. The optimum impedance realization is shown in Fig. 12. EM model successfully realizes impedances. Matching networks should be low loss and evaluated in 50 Ω system.

$$I.L.(dB) = 10\log\left(\frac{1-|S_{11}|^2}{|S_{21}|^2}\right) \quad (6)$$

where S_{11} and S_{21} are [S] parameters of the network. The matching networks have acceptable losses that is indicated in Fig. 13. At 2.1 GHz, the input matching circuit exhibits a loss of 0.2 dB and the output matching cuicuit has a loss of 0.3 dB. Their values are acceptable. After correctly designing all parts of the PA, the final circuit will be evaluated. The final circuit schematic, is depicted in Fig. 14. Other circuit components such as the DC-block capacitor and RF-bypass capacitor, are replaced with the commercial models provided by Murata (Murata Manufacturing Co.). The bond-wires use default in the ADS library.

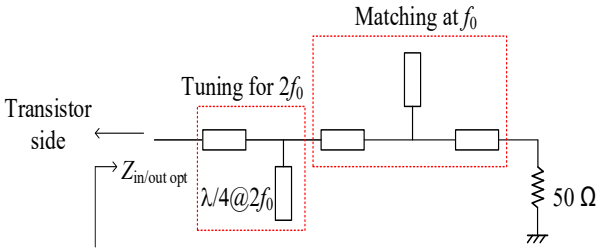

Fig. 10. Matching networks design strategy

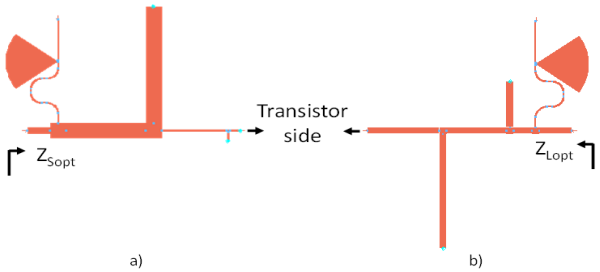

Fig. 11. Layouts of input matching circuit (a) and output matching circuit (b)

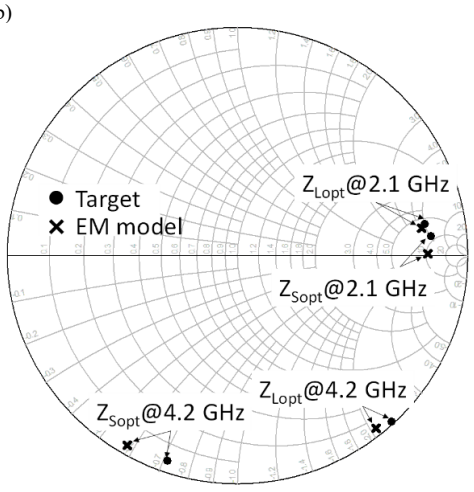

Fig. 12. Realized impedances by the designed matching circuits

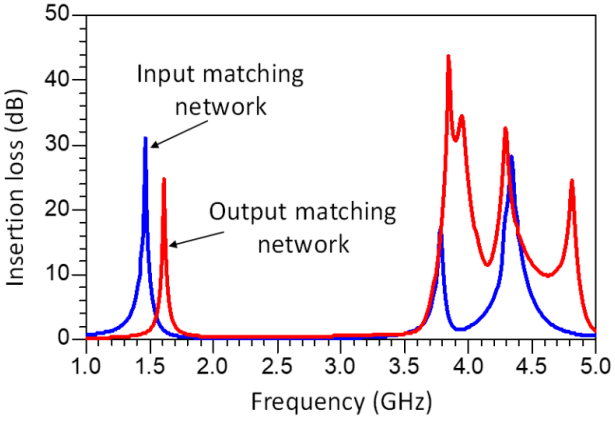

Fig. 13. Losses simulation of the input and output matching circuits

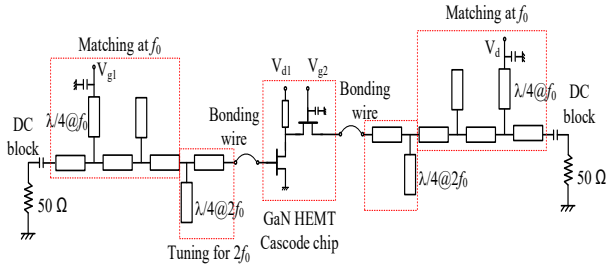

Fig. 14. Final circuit schematic

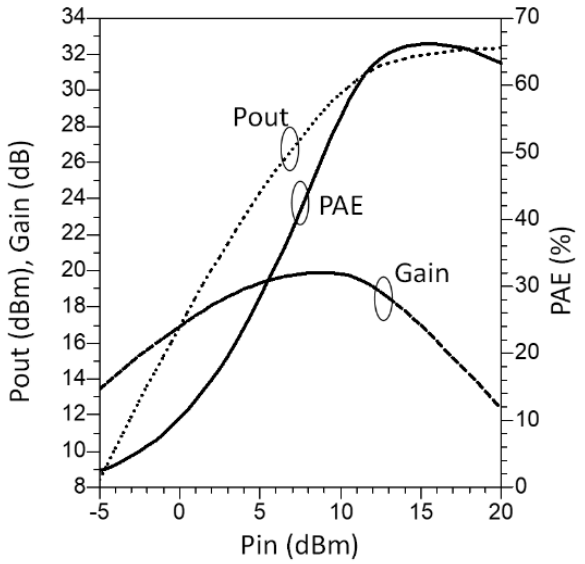

Fig. 15. Simulated transfer characteristic at 2.1 GHz

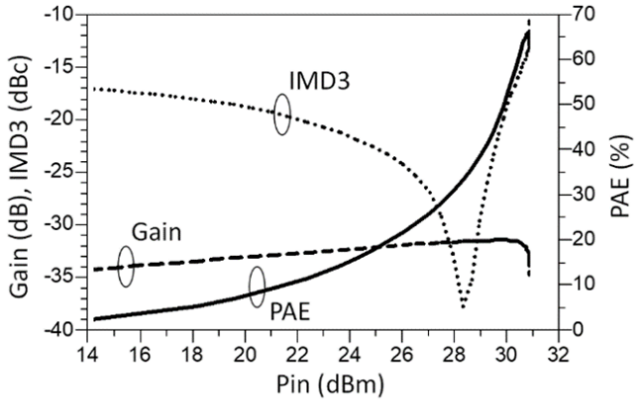

Fig. 16. Simulated IMD3 and Gain at 2.1 GHz

3.4. Simulation results

The one-tone and two-tone simulated results of the proposed PA are shown in Fig. 16 and Fig. 17. Fig. 16 indicates the one-tone operation, where the designed PA delivers a PAE of up to 66 % and a 16.5-dB Gain with a 32-dBm output power. Fig. 17 shows that for two-tone operation of a 4-MHz spacing, the designed PA delivers a 19.7-dB power gain, PAE of 35.8 % and an -35-dBc IMD3 level. These simulated results validate that the designed PA can offer both good efficiency and linearity.

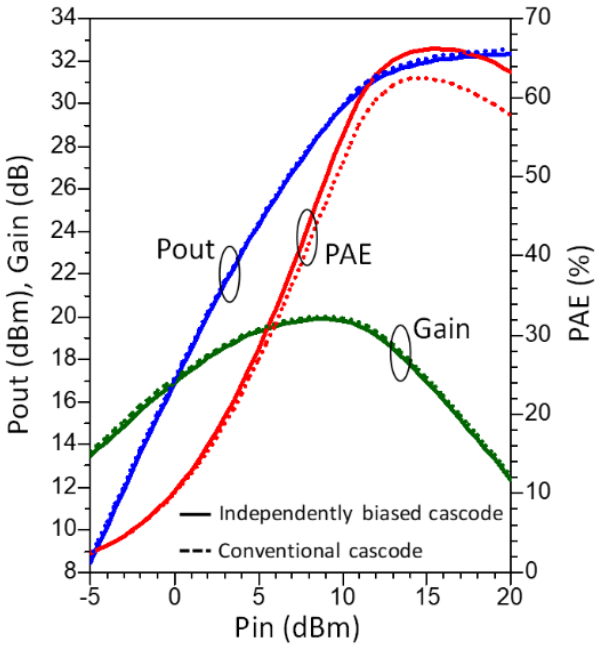

Fig. 17. The proposed circuit in comparison with the conventional one in one-tone operation

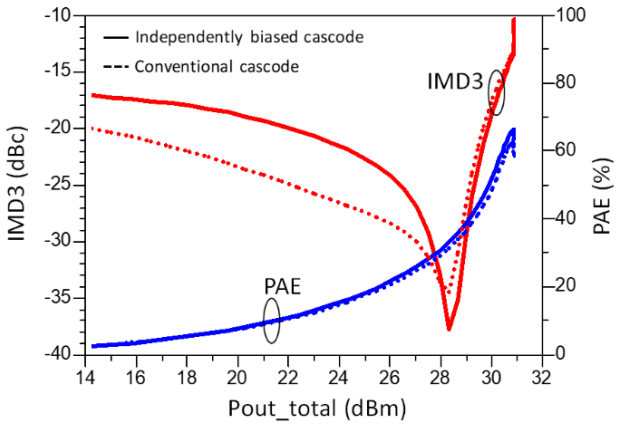

Fig. 18. The proposed circuit in comparison with the conventional one in two-tone operation

To further validate the promising advantages of the proposed PA in terms of linearity and efficiency, the following figures show a comparison of the simulated linearity and efficiency between a conventional PA and the proposed PA. The conventional one is implemented by removing the additional bias terminal while keeping the bias condition. The comparison between the two PAs are indicated in Fig. 17 and Fig. 18. In Fig. 17 showing the one-tone performance comparison, although power gain and output power are the same, about 4% higher maximum PAE of the designed PA than the conventional can be seen. Additionally, from Fig. 18 showing two-tone performance comparison, the designed PA offers lower IMD3 level with a

higher efficiency. Importantly, at -35 dBc IMD3 level, the proposed PA has a 5.8% better efficiency than the conventional PA. This confirms that the proposed circuit topology can offer good linearity as well as efficiency over the conventional circuit.

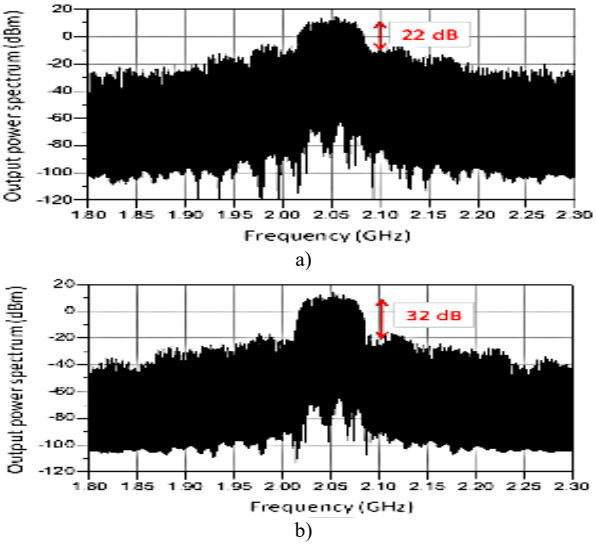

Fig. 19. Simulated ACPR comparison between the two configurations

Fig. 19 describes a comparison of ACPR, which is a critical metric for modern wireless communication systems. A Quadrature Phase Shift Keying (QPSK) modulation format with a center frequency of 2.05 GHz and a bit-rate of 100 MHz is employed for the ACPR simulation. The output power spectrum of the two PAs using this modulation format is indicated in Fig. 19. As can be clearly seen, the ACPR of the proposed PA (32 dB) is significantly higher than the conventional PA (22 dB). Here, it is worth noting that a carrier frequency of 2.05 GHz is used instead of 2.1 GHz due to a convergence issue in Harmonic Balance analysis in the ADS simulator. This result has further validated the advantage of the designed PA in terms of linearity.

4. Conclusions

This paper introduces an a novel GaN HEMT circuit to improve the linearity as well as efficiency of the PAs. It was found that the first drain bias voltage Vd1 contributed mainly to the circuit's performance improvement. Thanks to the adaptive control of operation condition for each transistor, the designed PA can be used for high efficiency or high linearity operations. When operating with the one-tone condition at 2.1 GHz, the designed PA delivers a maximum efficiency of 66%, 16.5-dB gain, and 32-dBm output power. For two-tone operation, it delivers a PAE of 35.8%, IMD3 level of -35 dBc and 19.7-dB power gain. Compared with the conventional circuit, the proposed PA delivers better linearity as well as efficiency

Acknowledgements
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