Journal of Engineering Science and Technology Review 16 (2) (2023) 207 - 213

Research Article

JOURNAL OF
Engineering Science and Technology Review

www.jestr.org

Predictive Power Control Circuit Model With T-DET-FF for Hybrid Pulsed Latch Implementation

Sharath Chandra Inguva[1,*], B. Mythily Devi[2], Anitha Bujunuru,[2] R. Shashikala[2] and O. Ravinder[2]

[1]*Department of Electronics and Communication Engineering, Matrusri Engineering College,Hyderabad, Telangana, India.*
[2]*Department of Electronics and Communication Engineering, Gurunanak Institutions Technical Campus, Hyderabad, Telangana, India.*

Received 24 April 2022; Accepted 12 February 2023

Abstract

Pulsed Latches circuits are one important aspects of the reduction of power for each read and write operations in memories. As the design complexity with reduction of nanometers increases the design analysis on power and other performance factors with relate to foundry techniques encapsulated in Semiconductor gates. With importance of low power feature in memories are implied with reduction of size of the transistor and its implementation with type of application chosen. In this paper, we implicate on the feature of power reduction models with a hybrid feature of T-DET-FF modelling with PPC circuit design using transistor gates. With regards of the power and the transistor size the proposed algorithm sufficiently provides the values W/L ratio to implicate the different conditions for Pulsed latches for memory write and read conditions. The simulated results with D-T-FF are implicated with Dynamic CMOS latch with PPC circuit as the comparison of different foundries with 32nm, 45nm and 65nm.

Keywords: DETFF (dual edge triggered flip flop), MOSFET (Metal Oxide Semiconductor Field effect Transistor), CMOS (Complementary effect Transistor), FF(Flip flops), DSA (Dual Sleep Approach), true single phase clock (TSPC)

1. Introduction

Flip-flops are now commonly utilized for information storage in VLSI design, and they have a long history of usage. When it comes to flip flop performance and fault tolerance, the speed, power consumption, and dependability of the device are all critical factors to consider. Therefore, it is critical to design flip-flops with the least amount of power consumption, propagation delay, and area while providing the best level of dependability and fault tolerance capabilities. As shown by the most recent research, device scaling reduces the supply voltage and device capacitances in digital VLSI designs, making the circuit more vulnerable to glitches. As soon as particles come into contact with the drain side of a MOSFET, electron hole combinations are formed. An induced drift transient current is produced by the opposite biased electric field [1-2]. A transient fault is defined as a voltage transient that occurs as a consequence of the accumulation of charge. Memory circuits may suffer from transient failures as a result of the combinational circuit glitches that have occurred before. Supply voltage scaling may be used to achieve low power usage in an efficient manner. Since a percentage of overall electricity usage, power consumption due to glitches cannot be ignored, as the percentage ranges from 9 percent to 38 percent [3]. At the moment, one of the most difficult challenges for researchers working on integrated designs is the construction of energy efficient circuits [4]. Latch designs that lower average power consumption as well as power delay product were provided in [5- 6] by the authors (PDP). [7] It is possible that the clock distribution network consumes around 45 percent of the overall system power. Because a clock network uses more power than a single clock, it is necessary to reduce the overall number of clocks. With the basic registers, the true single phase clock (TSPC) technique has been recommended in order to reduce the number of clocks [8]. It is possible to reduce the frequency of the clock and hence reduce its power consumption by sampling the input data on both the rising and falling edges of the clock, without affecting the system throughput. The DET technique reduces the clock network system's half-power usage to the bare minimum. Despite the fact that DET circuits are more sophisticated than SET circuits, they have the potential to be more energy efficient [9].

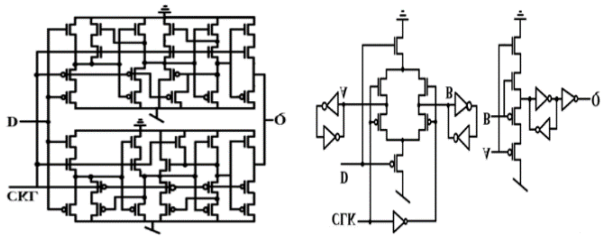


Fig. 1. Representing the Existing Glitch free CMOS model based on DET FLIP FLOPS.

2. Existing Design DET –FF Models and Description:

In [15], the suggested design was upgraded using common Latch-MUX DET flip flops, which have the advantage of its internal circuit no necessarily never changes in response to changes in the input signal, as opposed to previous designs. As per the design model in [15], the energy models and its estimation as measured with circuit design based on the MUX-latch Flip flop with a dual edge triggered circuit. The glitch conditions are observed at input nodes with circuit designed in [15]. Similarly, in Fig-2, a circuit model with

*E-mail address: sharath.inguva@gmail.com
ISSN: 1791-2377
doi:10.25103/jestr.162.25

glitch free design indicating the transistor implementation with PMOS and NMOS circuit where the switching activity are implicated with three level C circuit design. The C element circuit is the bridge circuit estimated with 3 PMOS and 1 NMOS from the Fig-2 with the cascading combination of pull-up or pull down transistor logic.

This study of the C element circuit enables to choose the different transistor design model with active or saturation stages for the switch considerations which has been presented in [16]. Unlike other implementation of the designs the input D, clk and section at R, are improvised with NOT gate.

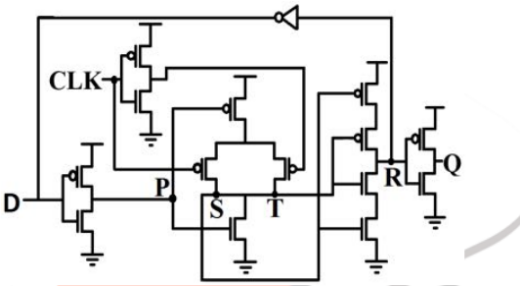


Fig. 2. Representing the final model for part (a) of DET FF for Glitch free design.

With the considerations of design of the C element circuits as differentiated with following features as:

- If the inputs are not equal, it is possible that the output will not reach the high impedance condition.
- Two transistors are used in the C-element circuit; however, three transistors are used in these configurations.
- This design with advanced feature for glitch reduction as per the DET FF has the potential to lessen the number of glitches that may develop at the input node as a result of the preceding circuits in Fig-3.
- In addition, this design minimizes the device's latency and average power consumption while simultaneously increasing its speed [17],[18],[19].

To attain compact area, low power, and high speed in the realm of VLSI design, academics are focusing their efforts today on achieving these goals. As a result, many additional techniques to achieving the goal have been proposed by researchers working on VLSI applications. As seen in Fig.4, the Glitch Resistant Dual Edge Triggered Flip Flop (GR-DET-FF) circuit has been designed. Using the proposed circuit model saves power and ensures error-free output. How does this design work?

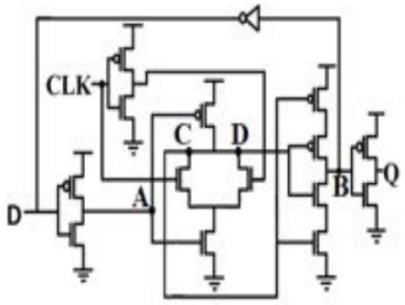


Fig. 3. Representing the final model for part (b) of DET FF for Glitch free design.

Here's how it works: There are two possible outcomes for the glitch in case 1: Either it is filtered out or it propagates to the output node Q and is then removed by feedback in case 2, as previously mentioned. Nodes A and B's beginning states are A=B=0, C=D=1 and Q=1 and clk=0, whereas nodes C and D's initial states are A=B=0. The value of the node A will change from 0 to 1 if any glitch occurs as a consequence of the preceding combinational circuit, and the value of the node A will change back to 0. The first 1P-2Nstructures yield C=0 now that A=1 and clk=0 have been established. The second 1P-2N structure has an output D=0 since A=1 and clk=1. C and T are now equal. Consequently, the C-element circuits output is B=0, and the Q-element circuits output is Q=1. As a consequence, the output device remains in the same condition. For the sake of argument, let's assume that nodes A and B are initially in the states of A = B = 1, C = D = 0, output Q = 0, and clk = 0, and that node C is initially in the state of A = B = 1. It is possible that the node A value will change from 1 to 0 if a problem develops there. The original 1P-2N structure uses A=0 and clk=0. Because of this, C=1 is correct. When A=0 and clk=1 are used as inputs to the second 1P-2N structure, the output goes to the high impedance state, implying that it is in its previous state, D=0. No change in output state now that C=1 and D=0, B=1 and output Q=0 are also connected to the high impedance of the C-element circuit. Errors in input are not handled, hence they have no effect on the system's time, space or power consumption. Since it is completely glitch-proof, quick, and efficient, the new GR-DET FF design described here is a significant improvement over prior designs.

3. Proposed design for ppc-d-t ff

The impact of PPC algorithm from the equation of I_d would effective suffice the power leakage factors and its estimation on the Hybrid D-T flip flops. In PPC algorithm, we improvise the equation I_d with V_{gs}, V_{dd} and $\frac{W}{l}$ $ratio$ with formulation mentioned below:

$$I_{dpresat} = K * \frac{W}{l} * (V_g) - V_{on} * V_d - \frac{V_d^2}{2} \quad (1)$$

$$I_{Dsat} = K * \frac{W}{l} * V_g - V_{on}^2 \quad (2)$$

$$I_d = \left(\frac{1}{I_{dsat}} + \frac{1}{I_{dpresat}}\right)^{-1} \quad (3)$$

The term predictive is withheld on the design feature where rate of I_d is estimated with stochastic random probability model for each set transistor logic design based on the circuit diagram. Let us assume the rate is of each transistor is consistent with voltages are considered at one particular value for each section of Transistor considered. So, the voltage at ON condition and input voltage at gate becomes constant.

Now, we improvise an algorithm with power prediction feature control from the conditions stated below:

- Let P_d is power estimated at drain and P_o is the output power the proposed circuit on Hybrid-DT FF.

$Pd = V_d * I_d$ (4)

- With the equation 4 we improve a stochastic random probability for which P_d is minimum.

Since we know that $Power \propto Area$, hence the estimated area for a given circuit is obtained with expected probability of Power/Area that is governed with (2) and (3) as representing using Conditional expected probability:

$Let\ X, Y\ be\ the\ random\ variables\ for\ the\ Power\ and\ Area\ to\ initiate\ the\ different\ performamnce\ features\ models$

$$P\left(\frac{X}{Y}\right) = F(X) * \frac{P(X \cap Y)}{P(Y)} \quad (5)$$

Since X and Y being the power at drain and Area for which transistor logic is estimated with $\frac{W}{L}$ ratio chosen. Hence the rate of change of Power with area at drain will be minimum hence a constant value ε.

$$\frac{d}{da}(P_d) = \varepsilon \quad (6)$$

Hence from equations,

$$I_{dpresat} = K * \frac{W}{l} * (V_g) - \alpha \quad (7)$$

$$I_{Dsat} = K * \frac{W}{l} * V_g - \beta \quad (8)$$

Finally, we substitute the design equations of 7,8 in 3 we have,

$$I_d = \frac{\left\{\left(K*\frac{W}{l}*(V_g)-\alpha\right)+\left(K*\frac{W}{l}*(V_g)-\beta\right)\right\}}{\left(K*\frac{W}{l}*(V_g)-\alpha\right)*\left(K*\frac{W}{l}*(V_g)-\beta\right)} \quad (9)$$

$$\frac{d}{da}(I_d) = \varepsilon \quad (10)$$

From (6).

Hence solving the equation 9 with 10 we have,

$$I_d \approx e^{\frac{V_g}{W}*l-2*\alpha\beta} \quad (11)$$

Here $\alpha\beta$ provides the voltage at drain and ON condition of transistor. So the values estimated with I_d and V_{gs} values from each transistor with PMOS and NMOS length and width.

3.1. Power Leakage Reduction Models:

3.1.1. Transistor stacking (self-reverse biased)

When current travels through a stack of transistors that are coupled in series, the amount of subthreshold leakage current decreases. The transistor stacking method is shown in the following images. As a result of the tiny drain current flowing through M1 and M2, the voltage at the intermediate node Vm is positive when both M1 and M2 are switched off. Because of the positive source potential, the gate to source voltage of M1 becomes negative, resulting in a reduction in subthreshold current.

3.1.2. Sleep transistor technique

The sleep transistor strategy is the most widely used technology for reducing leakage power. It is also the most expensive. In this approach, an additional "sleep" PMOS transistor is inserted between the pull up network and the VDD, and an additional NMOS transistor is placed between the ground and the pull down network, resulting in a total of three additional transistors. This kind of transistor turns off the circuit by turning off the power while the circuit is in the sleep state. As a result, by switching off the power supply, this technology may significantly limit leakage power with a large margin of safety. However, when used in the sleep state, this strategy results in floating output.

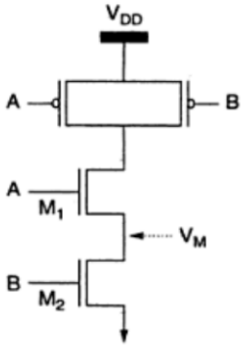


Fig. 4. Representing the self-reversed-biased circuit for power reduction.

3.1.3. Sleepy stack approach

Once the condition for sleep transistor concept is successfully integrated with the stack solution, this sleep stack approach is established. This model utilizes, the design with

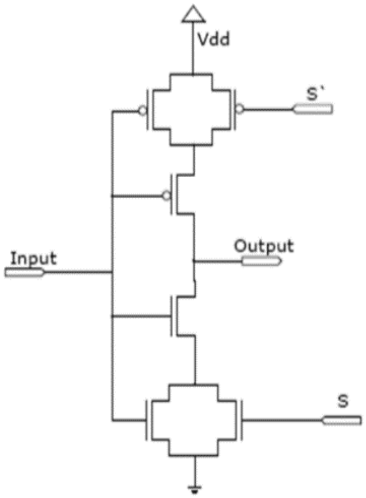


Fig. 5. Representing the sleep transistor circuit for power reduction.

Once this is done, one of the split transistors is linked in parallel with one of the sleep transistors. During the sleep mode, sleep transistors are turned off, and the leakage current is reduced by stacking transistors. The most significant disadvantage of this procedure is the power delay, which occurs since we are changing the transistors.

3.1.4. Sleepy keeper approach

In sleepy keeper technique, sleep transistors is parallel in both pull up and pull down network. It uses the leakage feedback technique.

Pull up and pull down networks are connected in parallel in a sleepy keeper strategy, and the same is true for the pull up and pull down networks. The method of leaking feedback is used.

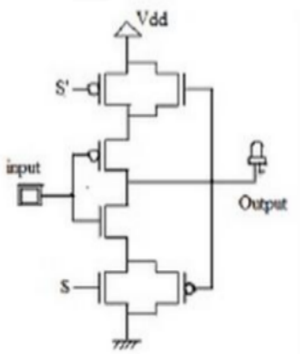


Fig. 6. Representing the sleepy keeper circuit for power reduction.

In this technology, a PMOS and an NMOS transistor are put in parallel with one other. In sleep mode, sleep transistors are switched off, and one of the parallel connected transistors is kept connected to the track power rail throughout the sleep period.

3.1.5. Dual-Sleep Approach

Two transistors are connected in parallel when employing dual sleep strategies, comparable to the keeper method. In both active and inactive modes, sleep transistors are always connected to both the pull-down and pull-up networks.

GND and VDD are always connected to the output. This approach uses fewer transistors than the previous one to create a certain logic circuit. A great balance between power, delay, and area may be achieved by using this method.

3.1.6. Dual Stack Approach

Two PMOS transistors and two NMOS transistors are utilized in the dual stack approach. When it comes to the pull down network, two PMOS transistors are employed, whereas two NMOS transistors are used in the draw up network.

NMOS degrades at high logic levels, while PMOS degrades at low logic levels. This approach has the benefit of being more efficient. However, one of the downsides of this strategy as compared to the prior technique is that the wait is longer.

3.1.7. CMOS with variable threshold (VTCMOS)

This is an example of a design method known as body biasing. Body bias is controlled using a self-substrate bias circuit, which allows for the achievement of various threshold voltages.

To manage the threshold voltage and cut down leakage current in the active mode, a zero body bias is applied, but in the standby mode, a reverse body bias is used to achieve the same results.

3.2. Design Procedure and its objectives

- To analyze and implement the H-D-T power control circuit.
- Analyzing the current design model and its limitations as a constant of power case in micro wind software.
- Hybrid scenario of the design circuit and its power reduction algorithm for the current design approach.
- Emphasizing on the PAD {Power, Area, and Delay} model to ensure the design.

3.3. Design Circuit Diagram and Its Implementation

The design and its feature model would suffice the requirements on the power calculation and leakage requirements for each set of the circuit changes. We propose a hybrid approach and reduced W/L ratio to realize the change of the each parametric change occurred in the designed circuit model. Our design approach improvises on the novelty of power reduction as its shows nearly zero watts of power for the CMOS - {NOT} feedback as mentioned in circuit model.

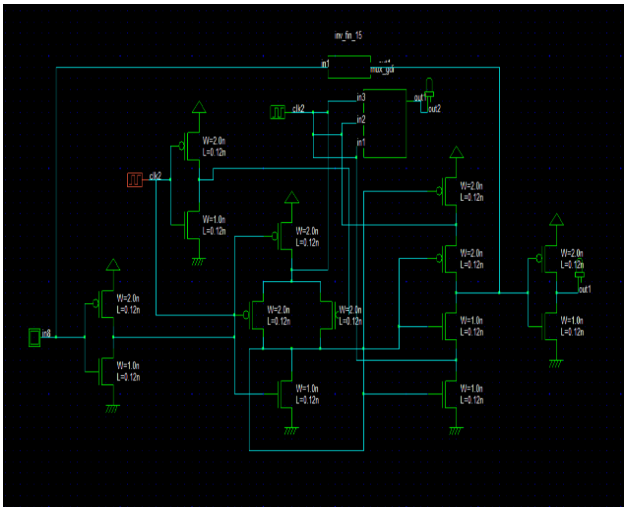


Fig. 7. Representing the proposed design I circuit schematic for Glitch free design.

The current design model aim to improve the circuit functionality and its parametric criteria on each section of the design block unit as mentioned below:

1. Improvising the pull up and pull down model for the Edge triggered criteria on each transistor phase of design.
2. Not gate implementation with edge triggered and button triggered.
3. Description of each model and its implementation using Power reduction analysis.
4. The current design aims to introduce four variations and its implementation characteristics with the PMOS and NMOS gate. W/L is one such factor which improvising the technology parameter initiating the difference in design model and its structural changes in regards with power and area.

Conditional changes in the circuit (in regards to change in W/L) would suggest the different input variations as mentioned. Our design aims to change design model which utilized less power and have to implement a power reduction technique. As per the above mentioned power reduction techniques we have modelled a hybrid scenario of the design as a combination of sleepy stack and dual stack approaches to ensure less delay and less power.

This design model improvises on the three different scenarios where each section happens to provide data to pull and pull down transistor as mentioned in below figures.

Each such transistor phase would represent the data which are either placed horizontally or bridge connections using wheat stone connection where the over voltage drop would be zero.

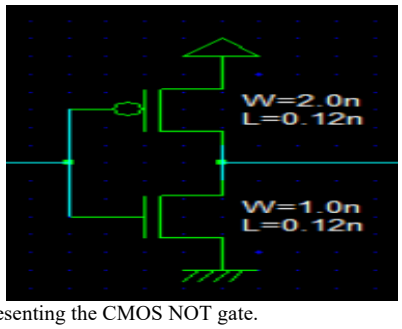


Fig. 8. Representing the CMOS NOT gate.

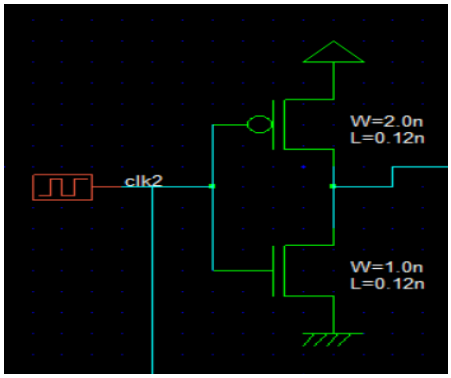


Fig. 9. Representing Edge triggered NOT gate.

The bride connection would suffice with 1 NMOS and 3 PMOS transistor for regulating the output either zero or 1 at each output phase.

The given data is regulated with the input button and clock for not gate, hence regulating only one set of transistor are utilized as pair (1NMOS-1PMOS).

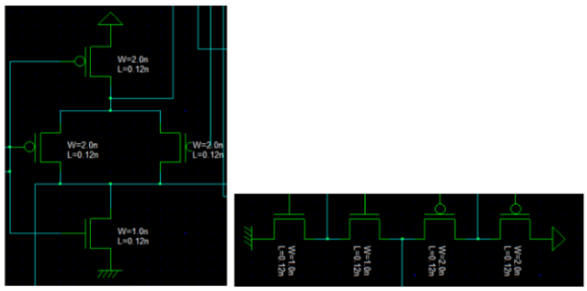


Fig. 10. Left: representing the bridge connection Right: Representing the parallel connection **.**

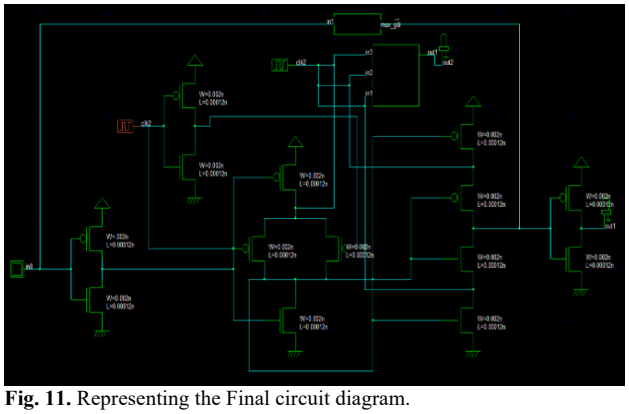
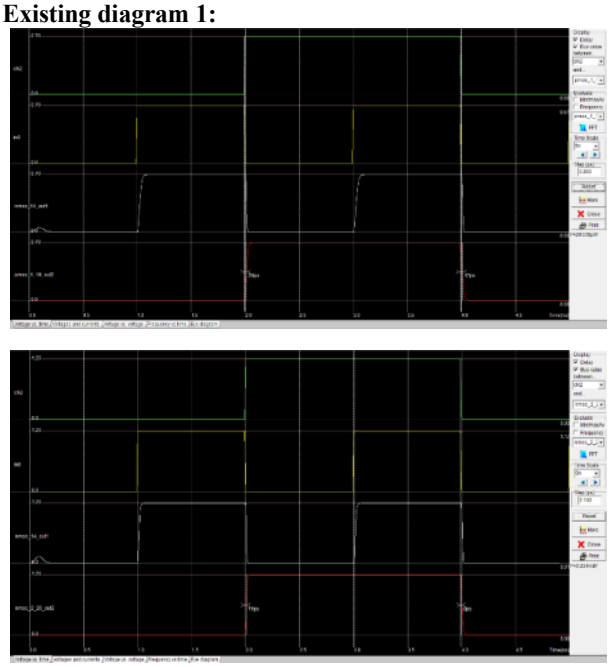


Fig. 11. Representing the Final circuit diagram.

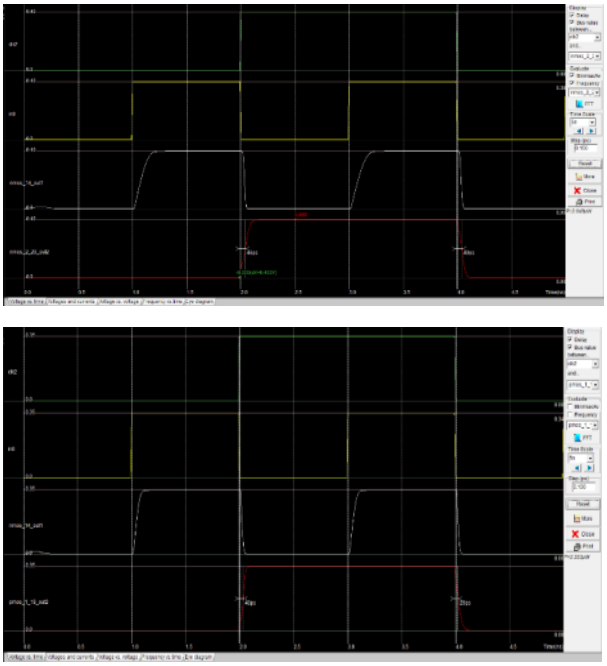
The current figure above would represent the circuit for the final conditions which are sequenced with 3 stage model as 2-not-gates, edge not gate, bridge pull up, pull down circuit and finally the comparator model with edge triggered. This circuit provides the effective low power circuitry and design challenges to current design estimation of the power reduction technique. As the input sequence with 011or 100 or 111 would result in change of the data ensuring the toggling of the inputs to comparator.

4. Results and Discussion

Existing diagram 1:



(a)



(b)

Fig. 12. (a) Representing the Existing Circuit Diagram 1 in 45 and 32 nanometer technology, (b) Representing the Circuit diagram 1 in 65 and 90 nanometer technology.

1. The existing two circuit models are represented with the circuit diagrams mention above resulting the schematic view and layout outputs.
2. Each circuit has small different with pull up and pull down scenario considering the design analogy
3. The power suppression with the proposed circuit has happened with each set of the nanometer technology utilized for the designed circuit diagram as mention below in tabulated.
4. At start of the design phase on each nanometer reduction we have observed subsequent changes and its reduction due to 3:1 P/N ratio and W/L is 1:125.
5. Considering these factors we have observed the design case and its relative analysis on the flip flop with both functionality of T and D.
6. Hence from the comparison table the proposed model have proven better results up to 20 % improvement factor in Area, 40% for power and 10 % delay improvement in 45 and 32 nm.

The current design encapsulates the design model and its features using M/L ratio and proposed NOT gate implementation with least power assigned while simulating the design. Ensuring the analysis of the design specifically related to the existing model where the P/N ratio is 1:2 at each design section of the pull up or pull down transistor. We have improvised a 3:1 ratio of P/N scenario with less W/L about 1:125 ratio resulting more than 10% change in all power, area and delay.

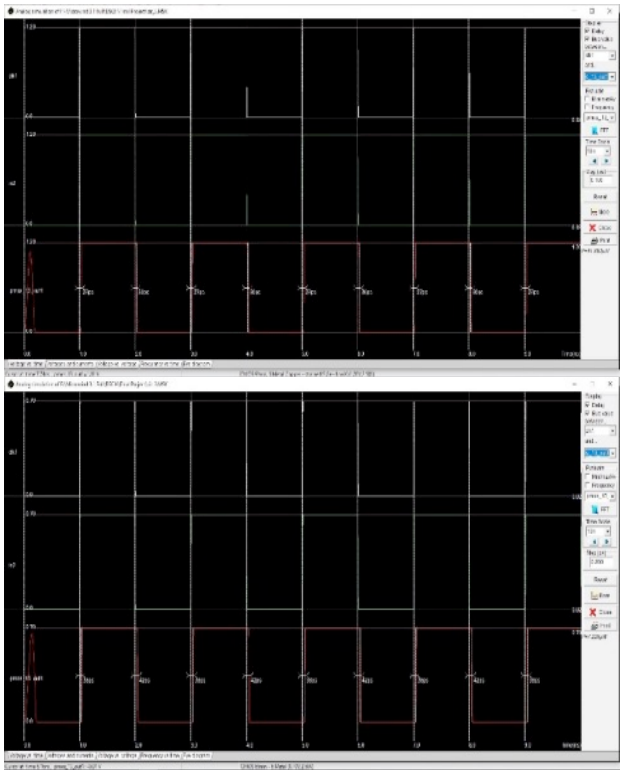


Fig. 13. Representing the Existing Circuit Diagram 2 in 45 and 32 nanometer technology

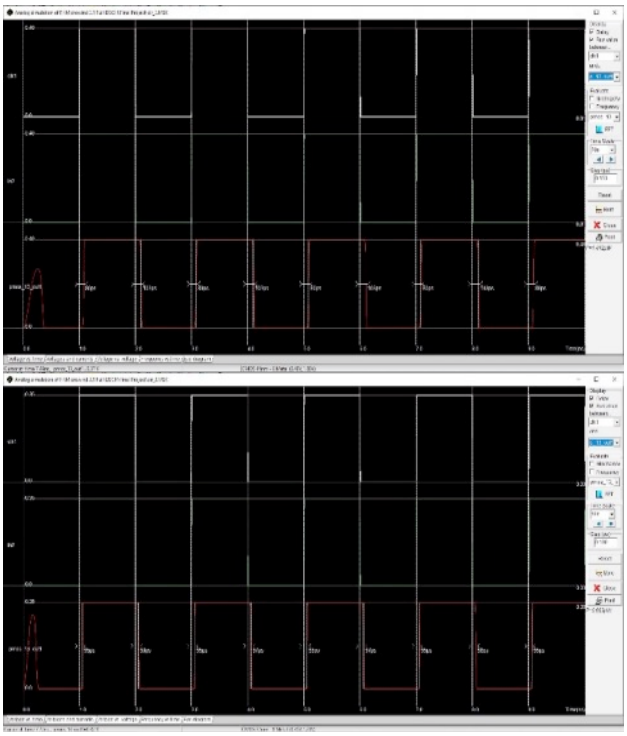


Fig. 14. Representing the Existing Circuit Diagram 2 in 65 and 90 nanometer technology.

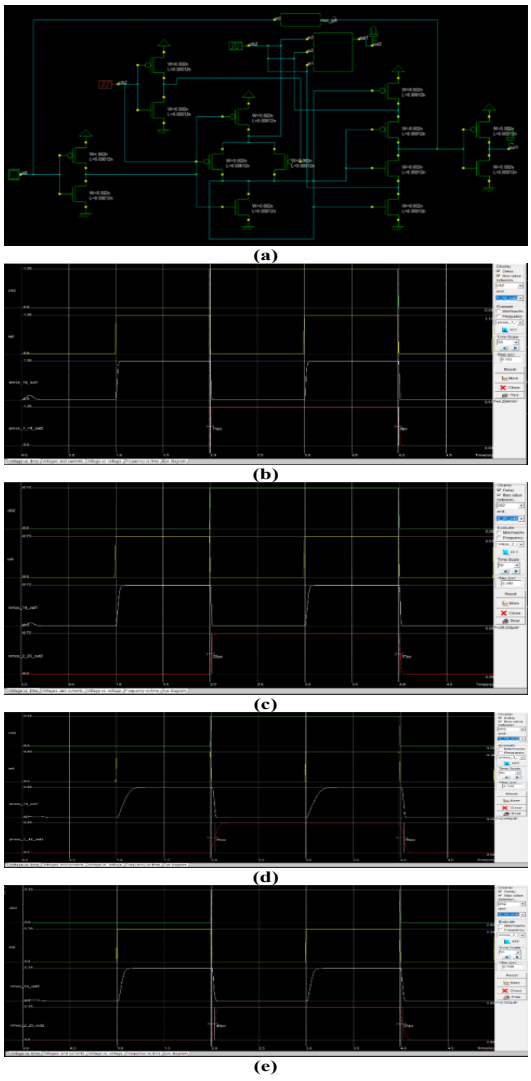


Fig. 15. (a) Representing the Proposed Circuit Diagram, (b) Representing the Existing Circuit Diagram 2 in 90 nanometer

technology, (c) Representing the Proposed Circuit Diagram for layout model in 65 nanometer, (d) representing the Proposed Circuit Diagram for layout model in 45 nanometer, (e) Representing the Proposed Circuit Diagram for layout model in 32 nanometer.

5. Conclusion

Since the design feature improvises a low power implementation with pulsed latches and flip-flops on the design perspective which effects the power control model and solution analysis with equation (11). The proposed design hasintegrated the 3P-1N structure with the bridge element circuit in order to boost performance even more. In order to lessen the input loading, the two structures are combined in order to share transistors that are linked to the data input. When compared to the previous DET-FF designs that have been explored, the suggested TET-FF has the lowest power consumption and the lowest power distribution point (PDP). The suggested design uses the minimum amount of transistors, which results in a tiny footprint and the shortest delay, which allows it to operate at high speeds and with great efficiency.

Future scope

To improvise an N-bit Flip-Flop with front end modelling with a low voltage control apart from current control model. To facilitate the design with low foundry technologies in Tanner EDA.

References

1. C. Augustine et al., “Characterization of PVT variation andaging induced hold time margins of flip-flop arrays at NTVin 22nm tri-gate CMOS,” in *Proc. IEEE Int. Electron DevicesMeeting (IEDM*), San Francisco, CA, USA, 2016, pp. 35.5.1–35.5.4
2. Z. Chen, H. Wang, G. Xie, and J. Gu, “A comprehensive stochastic design methodology for hold-timing resiliency in voltage-scalabledesign,” *IEEE Trans. Very Large Scale Integr. (VLSI*) Syst., 26 (10), 2018. pp. 2118–2131.
3. Pascal A. Meinerzhagen , SandipKundu , Andres Malavasi, Trang Nguyen, Muhammad M. Khellah, James W. Tschanz and Vivek De, “Min-Delay Margin/Error Detection and Correction for Flip-Flops and Pulsed Latches in 10-nm CMOS”, *IEEE Solid-State Circuits Letters,* 2 (9), 2019, pp-147-150.
4. Byung-Do yang, "low-power and area efficient shift register using pulsed latches", *IEEE Transaction on Circuits and System-I: Regular Paper*s. 62(6), 2015.
5. H-S. Kim, J.-H. Yang, S.-H. Park, S.-T. Ryu and G.-H. Cho, "A 10-bit column-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs", *IEEE J. Solid-state Circuits*,. 49, (3), 2014, pp. 766-782.
6. D. Rennie, D. Li, M. Sachdev, B. Bhuva, S. Jagannathan, S. Wen, et al., "Performance metastability and soft-error robustness tradeoffs for flip-flops in 40 nm cmos", *Circuits and Systems I: Regular Papers IEEE Transactions,* 59(8), 2012, pp. 1626-1634.
7. K. M. Keerthi, K. R. Pasupathy and B. Bindu, "Design of FinFET based all-digital DLL for multiphase clock generation", *Proc. Annu. IEEE India Conf. (INDICON)*, 2015 pp. 1-4.
8. M. Huang, Y. Lu, S.-W. Sin, S.-P. U and R. P. Martins, "A fully integrated digital LDO with coarse–fine-tuning and burst-mode operation", *IEEE Trans. Circuits Syst. II Exp. Briefs*,. 63(7), 2016 pp. 683-687.
9. T. Fischer, S. Arekapudi, E. Busta, C. Dietz, M. Golden, S. Hilker, et al., "Design solutions for the bulldozer 32 nm SOI 2-core processor module in an 8-core CPU", *IEEE ISSCC Dig. Tech. Papers*, 2011 pp. 78-80.
10. B. Narasimham, K. Chandrasekharan, J. K. Wang, K. Ni, B. L. Bhuva and R. D. Schrimpf, "Charge-Steering Latch Design in 16 nm FinFET Technology for Improved Soft Error Hardness", *IEEE Trans. Nucl. Sci.*. 64,2017, pp. 353-358.
11. Y. Chen, W. Chan, W. Wu, H. Liao, K. Pan, J. Liaw, et al., " A 16nm 128Mb SRAM in High- \$kappa\$ Metal-Gate FinFET Technology with Write-Assist Circuitry for Low-VMIN Applications ", *IEEE Intl. Solid-State Cir. Conf Proc*.,2014, pp. 238-239.
12. B. Narasimham; K. Chandrasekharan; J. K. Wang; B. L. Bhuva, “Soft Error Performance of High-Speed Pulsed-DICE-Latch Design in 16 nm and 7 nm FinFET Processes”, *IEEE International Reliability Physics Symposium (IRPS)*, 2019, pp 1-7.
13. Ki-Chan Woo; Hyeong-Ju Kang; Byung-Do Yang, “Area-Efficient Bidirectional Shift-Register Using Bidirectional Pulsed-Latches”, *IEEE Transactions on Circuits and Systems II: Express Briefs*, 66, (8), 2019, pp. 1386 – 1390.
14. X. Zhang et al., "A 0.6 V input CCM/DCM operating digital buck converter in 40 nm CMOS", *IEEE J. Solid-State Circuits*, 49(11), 2014, pp. 2377-2386.
15. E. Consoli, G. Palumbo, Jan M. Rabaey and M. Alioto, "Novel Class of Energy-Efficient Very High-Speed Conditional Push-Pull Pulsed Latches", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,* 22(7), 2014, pp 10-18.
16. K. Singh, O. A. Rodriguez Rosas, H. Jiao, J. Huisken and J. Pineda de Gyvez, "Multi-bit pulsed-latch based low power synchronous circuit design", *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018 pp. 1-5.
17. S. C. Inguva and J. B. Seventline, "FPGA based Implementation of Low power CORDIC architecture," *2019 International Conference on Intelligent Sustainable Systems (ICISS)*, Palladam, India, 2019, pp. 389-395.
18. S. C. Inguva and J. B. Seventline, "Enhanced CORDIC algorithm using an area efficient carry select adder," *2017 International Conference on Intelligent Sustainable Systems (ICISS)*, Palladam, India, 2017, pp. 410-415.
19. Dr. Sharath Chandra Inguva & Dr. J.B. Seventiline Implementation of FPGA design of FFT architecture based on CORDIC algorithm, *International Journal of Electronics,* 108:11, 2018, pp. 1914-1939,