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Performance Improvement for the VSC-HVDC Transmission System under Cascaded A.C. and D.C. Faults

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Abstract

Regarding HVDC systems wherein the total isolation of the failed circuit is not a practical solution, AC/DC line faults on HVDC systems using Voltage Source Converters (VSC) are a significant concern. In the HVDC system, an insulated-gate bipolar transistor (IGBT) is employed because it can take a maximum current and is also used in many industrial applications. Faults in an HVDC system's rectification or inverter portion significantly impact system reliability. In the HVDC system, many failures are examined, including an actuator, controller abnormalities, malfunctions throughout the inverter unit, overheating, and a 3-phase short circuit. Usually, the most frequent faults in an HVDC system are pole-to-earth faults on the DC-bus and 3-phase to-ground faults (A.C. faults). This article presents a terrific fault-current controller (TFCC) to limit the D.C. and A.C. fault currents for more significant improvement of the system capability. This study examines the characteristics of the VSC-HVDC with a 2-level VSC-HVDC network during cascading faults (D.C. and A.C. faults) to truly comprehend the network under these kinds of faults. The proposed technique's performance is investigated and compared with the existing techniques. Then the findings are obtained using the MATLAB tool.

Keywords: VSC-HVDC transmission, IGBT, AC fault, DC fault, terrific fault current controller (TFCC), MATLAB tool

1. Introduction

In terms of failure susceptibility and security, they face substantial challenges, particularly in high-power circumstances. That is mainly owing to the scarcity of commercially available D.C. switchgear. On the other hand, the VSC-HVDC is getting more study attention because it offers higher flexibility and adaptability, which is ideal for renewable resources. Massive offshore wind power incorporation into onshore utilities, in which a stable D.C. connection is required, becomes a valuable property of VSC HVDC. Yang, J., et al. (2011) [1]. Current source converter-based HVDC and VSC-HVDC are the two parts of the HVDC transmission network. VSC-HVDC has unique benefits beyond CSC-HVDC, especially for marine structures, like compactness with adaptable real and reactive power regulation. If the electricity distribution distance exceeds 60–100 km, VSC-HVDC is a better realistic alternative for transferring offshore electricity onshore. Because of the small DC-side impedance, the current due to a fault rises to a great value in a short period. Security is an important field of research for meshed D.C. transmission. A quick and dependable protective mechanism is necessary to minimize the severity of malfunctions. Although a few VSC designs can manage dc-side fault currents, the technique has yet to be implemented in electrical transmission systems. Standard AC system protection approaches (like impedance relay) are ineffective for VSC-DC protection. Chang B. et al. (2017) [2] present point-to-point VSC-HVDC network security solutions that disconnect the faulty line through A.C. breakers and the complete D.C. system. Due to the substantial transmission capacities required in MTDC technologies, it was not a realistic solution. It became essential to promptly and securely locate and disconnect the only faulty line, thereby preserving the converter's critical power electronic devices and maintaining supply security. The use of D.C. breakers is to isolate a defective D.C. connection.

Nevertheless, developing these switches for high-voltage implementations was a task for decades because, unlike A.C. networks, D.C. networks don't have a fundamental current zero, so a circuit breaker had to drive the current to zero and waste the energy trapped in the inductor. Yeap, Y.M., et al. (2017)[3]. The fault features and cause assessment are required for adequate protection layout since the D.C. line failure will substantially impact the functioning of the VSC-HVDC. The restoration issue must be considered, particularly for overhead power lines, to determine whether the system can be quickly restored during a brief breakdown. Wang, P., et al. (2017).[4] The significant technical difficulty for MMC use in lengthy overhead transmission connections or D.C. networks is D.C. fault avoidance. There were three approaches to resolving this problem. Xu, Z., Xiao, H., et al. (2018) [5].

The first option is to turn off the power to the A.C. breaker. The benefits of this approach are its great technical maturity and outstanding financial sustainability. Most industrial VSC-HVDC installations employ this technology to resolve DC-line abnormalities. Because of the A.C. breaker's poor response, the system would take ages to restore from D.C. fault conditions.

Another alternative is to use a fault-limiting converter. Whenever the current going through the IGBT exceeds two times the rated capacity, converters will be disabled to avoid IGBT problems due to heating. A full-bridge MMC converter,

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for example, can generate reversed EMF to obstruct the fault current. With this technique, the speed of restarting transmission of power during minor D.C. faults is rapid. Nevertheless, more powerful electronic components can result in higher equipment expenses and power loss. The regulator relying on full-bridge S.M.s requires double the IGBT components as the half-bridge SMs MMC, and the power loss expands by around 100 present; the regulator depending on clamp-double S.M.s requires 1.2 times the IGBT components, and the power loss was boosted by approximately 34.8 %A third way of dealing with D.C. faults is to use D.C. breakers.

The VSC-HVDC transmission line utilizing two-level converters has significant conversion inefficiencies, and a large dv/dt necessitates the use of a specific transformer with high insulating requirements. G.P. Adam et al (2010)[6] Multilevel converters are utilised in the VSC-HVDC transmission network, which has common inefficiencies, lower dv/dt, and requires less insulation than two-level converters. Despite the current achievements of VSC-HVDC-based transmission networks, there remain concerns about their long-term viability. The behaviour of the VSC-ride-through HVDC to AC/DC disturbances has received attention.

So, this paper analyses and examines the performance of this research under these faults. The proposed approach's performance is compared to existing techniques, and the results are observed using the MATLAB tool. This article presents the TFCC to limit the D.C. and A.C. fault currents for the more excellent capability of the VSC-HVDC network. The addition of this work is designed as follows: section II clarifies the literature survey; section III describes the presented technique; section IV illustrates the result and analysis, and section V summarizes the complete research.

2. Literature Survey

Research by Hao, Y., Wang, Q., et al. (2018) [7]. This is a revolutionary, intelligent approach to the fault location. For collecting faulty characteristics using HHT, the method using single-ended observation effectively uses frequencies, duration, and energy. To calculate the fault length, the inputs to SVR include delay time and unique frequencies. The model's variables are optimized via cross-validation and compared with other algorithms. In addition, the fault location is identified using HVCR. The short circuit assessment of an offshore A.C. grid made up of wind energy linked by HVAC wires is presented. Raza, M. et al. (2018) [8]. The VSC-HVDC transmits the electricity produced on the offshore A.C. grid to numerous onshore utilities. VSC-HVDC installations regulate the offshore A.C. system with frequency and voltage droop regulation. Under short-circuit situations in the offshore grids, a coordinated control method for wind farms and offshore VSCs is intended to guarantee FRT without affecting stable operation. Rendo J. et al. (2019) [9] research provided a fresh reactive-power control technique for High Voltage Direct Current multiterminal systems with VSC-HVDC to increase transient response in power transfer networks. The suggested scheme utilizes localized readings to calculate a weighted average of the frequency detected by the HVDC system's VSC units within every conversion part. It presents a quick and easy hybrid current-limiting circuit (HCLC) consisting of a current-limiting inductance (CLI) with an EDC in parallel connection with CLI. CLI reduces the DCCB's capability as well as breaker speed requirements. Using EDC reduces stress on the DCCB's energy-absorbing component and speeds up fault current interrupting.

Liu, J., Tai, N., et al. (2017) [10]. Multiterminal VSC-based HVDC (VSC-MTDC) technology is presented in Kim, M.K. et al. (2017)[11]. As a CSC-OPF issue, the suggested technique decreases expenses and transmission loss. three innovative control modules for offshore wind facilities using VSC-HVDC connections are presented by Ndreko, M. et al. (2017) [12]. The purpose is to improve the HVDC systems and associated offshore wind plant fault-riding thought (FRT) capabilities in stable and unstable A.C. disturbances. The construction of a transient investigation method of the active SI-TFCC is described initially by Li, B., and Jing, F. et al. (2018),[13] followed by the VSC-HVDC network with active SI-TFCC implemented.

Furthermore, the technique for resolving the equivalent circuit's state equations was discovered. The effect of the metal oxide arrester's preventive Voltage on current-limiting work is investigated upon the foundation. Pei, X. et al. (2018) [14] Work provides a unique pilot-protection method in the VSC-HVDC system to avoid D.C. line failure in development owing to primary protection breakdown. The suggested protective method relies on modulus T.W. current properties. Firstly, the protective start-up criteria are built using the 1-status T.W. current angle's exact number. Then the faulty area is detected by comparing the phases of WTMM of the 1-status starting T.W. current to both D.C. line endpoints. Therefore, the defective line is chosen based on the polarity of the localized 0-status starting reversal T.W. current. A 4-terminal VSC-DC grid electromagnetic transient design was produced to assess the system pilot protection concept. Wang, D. et al. (2019) [15] proposed T.W. directional pilot protection.

Moreover, the report investigates T.W. propagation over HVDC-TL. Further, the research presents innovative fault direction discriminating criteria based on a combination of LCC-HVDC with VSC-HVDC instant power and current. A faulty pole criterion associated with positive pole current versus negative pole current was also suggested. Furthermore, using PSCAD/EMTDC, the LCC-VSC-HVDC transmission model is constructed. Li, B., Lv, M., et al. (2020) [16]. After a fault occurs inside the VSC-HVDC transmission network, the propagated features of the Voltage traveling wave are examined. An enhanced protection theory is given depending upon the Voltage traveling wave, including line parameters depending on the frequency. To avoid security from malfunctioning whenever the synchronizing clocks are out of synchronization, a solution that solely uses electrical values on both endpoints of the connection is examined.

3. Proposed Work

The critical issue regarding VSC-HVDC transmissions is that if the A.C. voltage crashes at the end of the connection due to a significant fault under one of the A.C. sides, the real power transmission and reactive power production capabilities of the system are significantly reduced. So, we propose the terrific fault current controller (TFCC) to enhance the transmission network against DC/AC faults. By employing our proposed approach, we effectively optimize the capacity of the VSC-HVDC transmission.

3.1. Modelling of VSC-HVDC

Figure 1 depicts the accurate VSC-HVDC network for investigation Song, J. et al. (2020) [17]. VSC is made up of 3 branches, each with two IGBT switches. A simple typical

model is created by separating the A.C. and D.C. sides. The A.C. end is represented by voltage sources in series with impedance (Thevenin's equivalent), whereas the D.C. end is represented by a current source parallel to a shunt capacitor. The electricity transmitted among the sides of AC/DC is influenced by the current basis on the D.C. side, which even assures the balance of the system's power.

Fig. 1. VSC-HVDC transmission network.

As a consequence of the D.C. current, the D.C. voltage could be represented as follows:

$$V_{dc} = V_0 + \frac{1}{C_{dc}} \int_0^t I_{dc} \quad (1)$$

Figure 2 depicts the corresponding design for a VSC on the A.C. side.

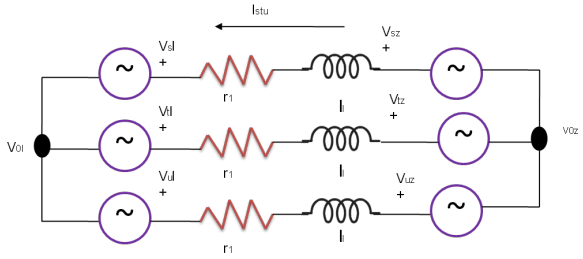

Fig. 2. Equivalent design.

3.2. The control arrangement of VSC-HVDC

It is required to add the Park transformation before implementing the control. The three-phase variables in the three-phase stationary structure (stu) are transformed into a two-phase synchronous reference structure using this transformation (qd). The real power is matched with the q-axis current element in the synchronized qd structure, whereas the d-axis represents the reactive power. The control scheme can be designed utilizing fixed amounts to control parameters on the rotating system that uses the Park transformation.

VSC controlling models are developed around a rotating qd structure. By controlling two electrical parameters in the qd frame, both VSCs in the system can regulate the real and reactive power flow separately. VSC endpoints could be employed in this point-to-point link to alter the power flow or D.C. voltage. In a qd structure, real and reactive power could be represented as:

$$\text{real power (P)} = \frac{3}{2}(V_q I_q + V_d I_d) \quad (2)$$

$$\text{reactive power (Q)} = \frac{3}{2}(V_q I_d + V_d I_q) \quad (3)$$

VSC uses a two-level cascaded regulator for its control structure. The A.C. grid current in the dq structure is regulated by the inner loop control design, whereas the D.C. voltage is regulated by the outer loop control design. One of several converters would manage the A.C. current flow, whereas the other maintains the DC-link Voltage in the VSC-HVDC link. However, rectification and the inversion units could be changed among these two controlling phases in the VSC-HVDC link. Consider the possibility of rectifier D.C. terminal overvoltage when employing the inverter to manage the D.C. voltage. The rectifier would use the primary control method mentioned above and then control the D.C. voltage in this research. In contrast, the inverter would solely use the inner loop control technique to individually manage the real and reactive power injection from the D.C. connection to the receiver end A.C. connection.

A two-level cascading system is used to control the rectifier. Figure 3 depicts the typical structure of the rectification end VSC.

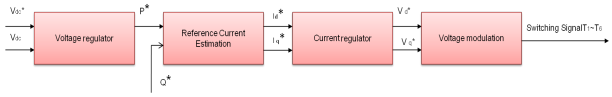

Fig. 3. Rectifier control.

The voltage regulator provides the real power reference signal in the VSC rectifier's controller design. On the other hand, the reactive power could be controlled to maintain the A.C. grid voltage. The reference signal Q* would be assigned to a fixed value.

Rather than regulating D.C. voltage, the inverter's control method would govern the real and reactive power supplied into the network. As a result, the inverter control doesn't need another voltage regulator. Figure 4 depicts the design of the inverter control.

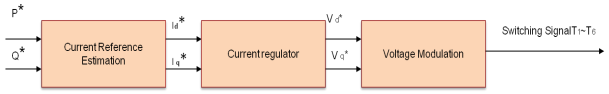

Fig. 4. Inverter control.

3.3. Outer control loop

The DC voltage converter is located in the outer circuit. The DC voltage regulator, shown in Figure 5, is responsible for maintaining the D.C. voltage at its set point (reference value) by guaranteeing that the power fed into the D.C. bus and injected into the A.C. system is balanced. The D.C. voltage converter uses a P.I. control approach with the input signal of observed D.C. voltage and its set point. The approach's outcome is the real power set point.

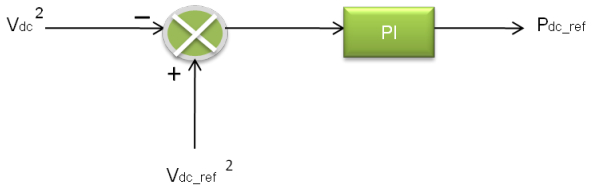

Fig. 5. D.C. voltage controller.

The set point of current could be calculated using the power set point via the easiest estimation:

$$i_q^* = \frac{2}{3} \frac{P^*}{V_{suq}} \quad (4)$$

$$i_d^* = \frac{2}{3} \frac{Q^*}{V_{suq}} \quad (5)$$

During a stable state, the d-axis element of the A.C. grid voltage should be zero if converted into a qd frame. Because the D.C. voltage is corrected in the rectifier by adjusting the real power, the active power responds. Only the standard

current I_q* must be changed in response to the real-time D.C. voltage observation. Regulating I_q* could be used to regulate the reactive power.
The voltage P.I. controller's close-loop transfer model can be represented as:

$$\frac{V_{dc}^2(s)}{V_{dc}^{*2}} = \frac{2s\xi_E\omega_E+\omega_E^2}{s^2+2s\xi_E\omega_E+\omega_E^2} \quad (6)$$

Gains on P.I. controllers could be formulated as having:

$$K_{p=C}\xi_E\omega_E \quad (7)$$

$$K_I = \frac{C\omega_E^2}{2} \quad (8)$$

$$Maximum\ peak\ overshoot\ (M_p) = 1 + e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}} \quad (9)$$

$$Settling\ time\ (t_s) = \frac{4}{\zeta\omega_n} \quad (10)$$

3.4. Inner control loop

The current regulator received the current set point. The current controller separates the d & q elements of current and Voltage as per the following equation. Figure 6 depicts the current controller.

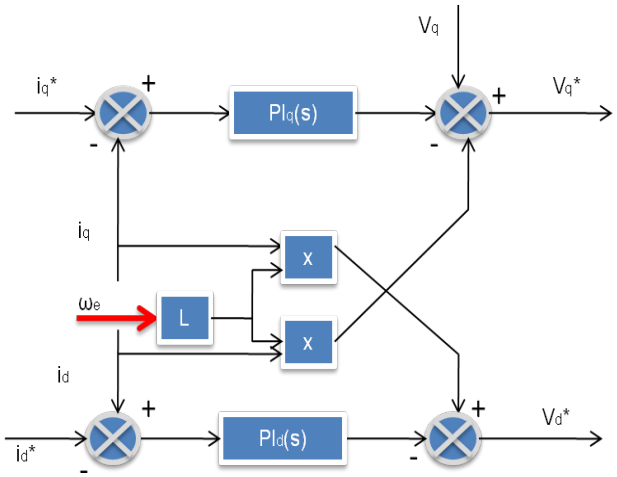

Fig. 6. A.C. current controller.

$$\begin{bmatrix} v_q^* \\ v_d^* \end{bmatrix} = \begin{bmatrix} r_l & 0 \\ 0 & r_l \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} l_l & 0 \\ 0 & l_l \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} \quad (11)$$

An "Internal Model Control Strategy" was created here to create the current controller.

$$K_P = \frac{l_l}{\tau} \quad (12)$$

$$K_I = \frac{r_l}{\tau} \quad (13)$$

Here l_l and r_l denote the inductor & resistor of the A.C. grid linked to the VSC, correspondingly.

The inverse Park transformation of qd elements could be employed to obtain the reference voltage in the $\{stu\}$ structure (V_{stu}^*) using the standard voltage value. To produce the switching signals of the 6-pulsed IGBT Bridge, the reference voltage would be delivered to the Voltage modulating circuit. The Pulse Width Modulation (PWM) technique is employed in switching signal-producing units. PWM modulates a switching signal having adjustable pulse duration by matching the standard voltage signal to a high-frequency triangle carrier signal.
Furthermore, measuring the A.C. grid voltage's rotating velocity requires the Phase-locked Loop (PLL) for accurate displacement monitoring.

3.5. Phase-locked Loop (PLL)

By calculating the electric degree and its angular velocity, the PLL is employed to provide the reference value for the conversion regulator to coordinate with A.C. voltage. A 3-phase PLL comprises a P.I. control and d-axis volt element feedback. The regulator's outcome is the power system's angular velocity. The electric degree may be found from the incorporation of the angular velocity. Figure 7 depicts the PLL mechanism.

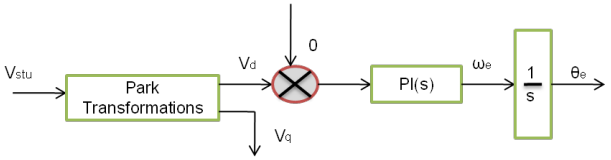

Fig. 7. PLL structure.

3.6. D.C. pole-to-ground fault

The principal effect of a pole-to-ground fault has been that the excellent pole voltage rises to two times its rated level. However, the A.C. side voltage does have a significant D.C. bias, which the transformer might not even be capable of handling. This poses a significant difficulty for transformer operation, including line insulation. The fault current of a pole-to-ground fault is lower than that of a pole-to-pole short circuit condition owing to the usage of small current grounded devices. The essential benefit is that every overcurrent wouldn't harm power equipment, and added security on bridge sections is unnecessary; unfortunately, it makes it hard to discover the fault. In reality, the controlling procedure could be sustained while active power swapped as planned as far as the conversion units are not tripped. As a result, these faults could be investigated in two phases:
Phase 1- Capacitor discharge: Since the DC-link Voltage doesn't fall to zero throughout this phase, thus freewheeling diode conduction never takes place.
Phase 2- Grid-part current supplying phase: This phase happens after the capacitance has discharged and its Voltage has dropped near zero.

3.7. A.C. faults

The DC voltage drops to a critically low amount as soon as an A.C. fault happens. This is because a neighbouring D.C. capacitance reacts by releasing current towards the fault location at that precise moment. The Voltage drops due to the current clearance, which even the DC-line appears to be experiencing. An increment in current must characterize a reduction in Voltage to keep the equal power. The available A.C. faults in the HVDC transmission network are listed below.

- The single line-to-ground (L-G) fault has been the most common type of fault inside the power system (about 80%), causing current and voltage circumstances to fluctuate at both the transmitting and receiving terminals. Users' voltage fluctuations and sags are to blame for this issue. It is most noticeable whenever a single phase-to-ground fault happens on the transmitting system's secondary side.

- A two-phase-to-ground fault: It causes the two-phase voltages to be the same, resulting in the system supplying severely imbalanced current and Voltage. The fault is introduced on the transformer's secondary. At the transmitting end, two-phase voltages become deformed, affecting the converter result on the D.C. transmission side. D.C. transmission lines benefit RMS voltage sag avoidance in terms of voltage recovery. Nevertheless, the voltage restoration time is too long relative to Ac systems.
- 3-phases-to-ground fault: It has been the most dangerous when contrasted with different faults. Whenever a three-phase-to-ground fault develops, the 3-phase voltages are zero when the fault is induced. Due to the obvious charging/discharging of capacitance, the resultant D.C. voltage wouldn't go to zero instantly. The receiving-end Voltage is unaffected by the L-G fault but drops dramatically in a three-phase-to-ground failure.

3.8. Terrific Fault Current Controller (TFCC)

Figure 8 depicts the unique TFCC's functional design. A current-limiting resistor (R_1), a high-speed regulated D.C. circuit breaker (K_1), a protective resistor (R_2), a metal oxide arrester (MOA) R_{MO}, and a current-limiting inductor (L_1) make up the majority of this system. Superconducting coils (SCCs) make up the inductor. The MOA is placed in shunt connection with the current-limiting inductor and could be employed to prevent switching overvoltage.

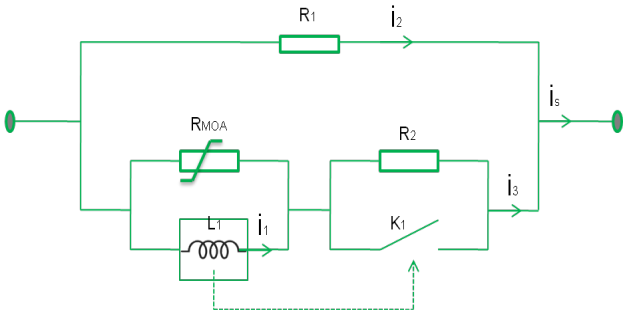

Fig. 8. Design of TFCC.

The structure of a VSC-HVDC transmission network incorporating TFCCs is shown in Figure 9; '$Z_{S.}$' denotes the circuit impedance.

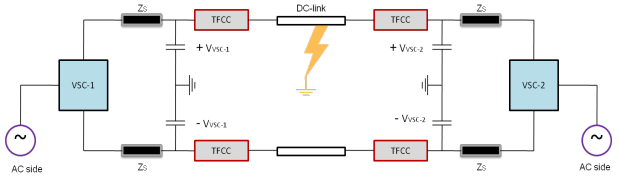

Fig. 9. Design of VSC-HVDC incorporated with TFCCs.

The TFCC process is depicted in Figure 10. Using the Voltage of inductor V_{L1} as detection signal V_{det}, an auxiliary controller gives a disconnected indication to the D.C. breaker K_1 whenever its level exceeds the specified threshold level. R_2 would be put into the connection while K_1 is unplugged to keep the SCCs' fault current underneath the significant level. Because the quenching of SCCs is prevented in this scenario, the TFCC's
dependability is enhanced. Next, determine if the DC-current line's level will be less than the security threshold level. If yes, the TFCC satisfies the current-limiting requirements, and the next stage is to detect and repair the fault. If that's not the case, the VSC-HVDC transmission network should be closed just at the rectifier-side unit to guarantee the network's security.

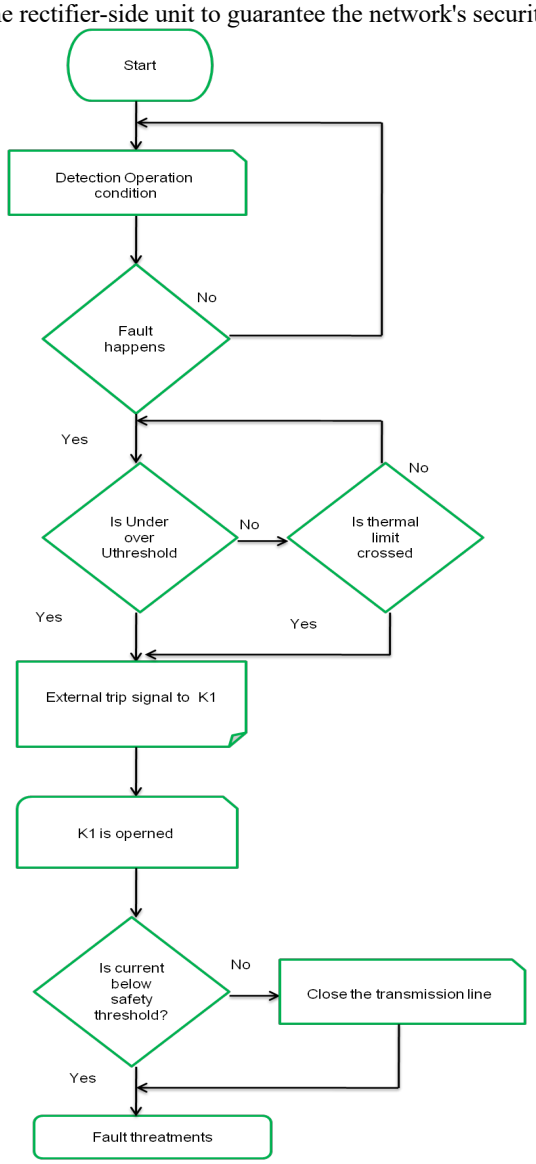

Fig. 10. TFCC process.

4. Result and Discussion

The VSC-HVDC network's dynamic properties were studied under various operational scenarios, including AC/DC faults, steady-state, variable D.C. power flows, and A.C. voltage. As a result, the D.C. and A.C. faults were introduced at the power system's transmission and reception terminals, and a fault assessment was conducted. MATLAB tool is used to simulate several simulated findings to discover the different fault features of the A.C. network.

4.1. Analysis of D.C. pole-to-ground fault

During DC pole-to-ground disturbances, the performance of 2-level VSC-HVDC is investigated. When a D.C. pole-to-ground fault happens, a large amount of excessive current is produced, resulting in a rapid drop in D.C. voltage. The freewheeling diode transmits the large A.C. grid current input into the D.C. fault, which could also harm the converter gate given the high fault current. Figure 11 shows the basic configuration of a 2-level VSC-HVDC network underneath a D.C. pole-to-ground fault on a DC-link.

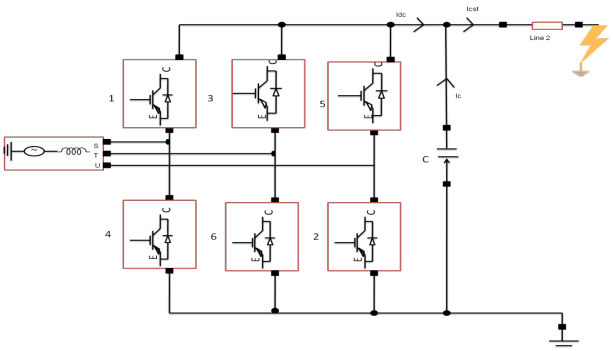

Fig. 11. Fundamental configuration of 2-level VSC-HVDC.

The modelling of a 2-level VSC-HVDC and the associated Voltage and current waveforms under proper usage are seen in Figs. 12 (a) and 12 (b) correspondingly. Whenever a pole-to-ground fault develops on the transmitting end of the Dc-link during t=0.08s, a voltage of the DC-link capacitor quickly drops, leading to a huge spike in D.C. fault current, and the fault is isolated within 0.01s, as illustrated in fig.12(c) and fig.12(d), correspondingly. The A.C. grid current input throughout a D.C. pole-to-ground fault enlarges the quantity of the fault current in the A.C. part, as depicted in fig.12 (e).

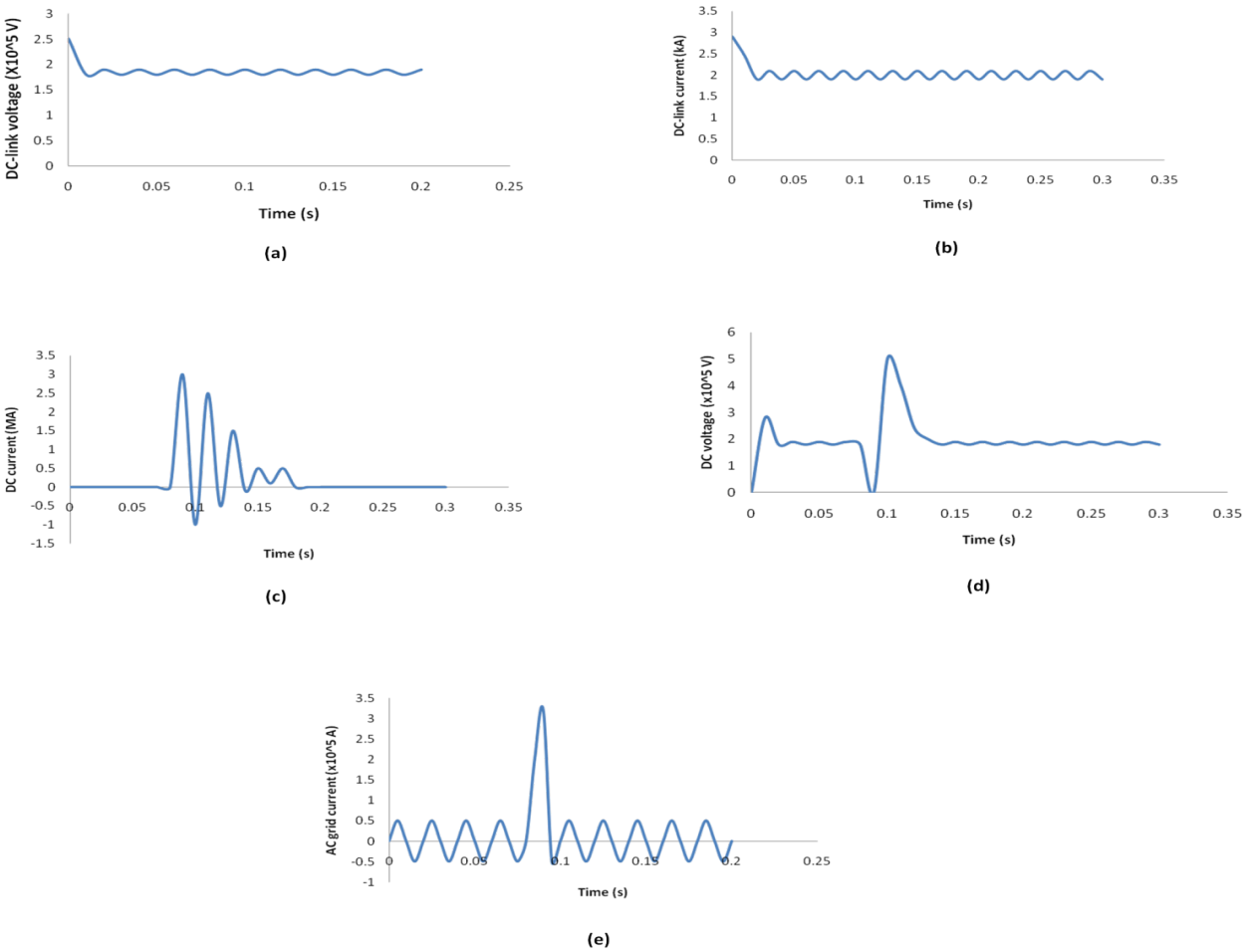

Fig. 12. Simulated outcomes of two-level VSC-HVDC (a) DC-link Voltage at the proper usage; (b) DC-link current at the proper usage; (c) D.C. current at the time of pole-to-ground fault; (d) D.C. voltage at the time of pole-to-ground fault; (e) AC-grid current at the time of pole-to-ground fault.

4.2. Analysis of A.C. fault

Figure 13 displays an HVDC transmission network focused on two-stage VSCs. These VSC-1/rectifier and VSC-2/inverter converters have been managed by 2.1 kHz switching frequency sinusoidal pulse width modulation (SPWM). On bus PCC-1, the rectifier adjusts real power & A.C. voltage amplitude. On bus PCC-2, the inverter modulates the dc-link Voltage with ac voltage magnitude. For PCC-1 and PCC-2, the real power instruction is responsive to voltage amplitude variations. As the voltage magnitudes of PCC-1 & PCC-2 decrease due to ac faults, this adjustment allows the rectifier to alter the real power instruction to cover the amount of transferable power. Consequently, our presented approach may avoid dc-link voltage increases by removing stored energy in the dc-link.

The maximum current input from the rectifier/inverter is restricted to the reactive current element, which corresponds to the converter's maximum reactive power capacity in the worst scenario, including a 3-phase fault at PCC-1 or PCC-2.

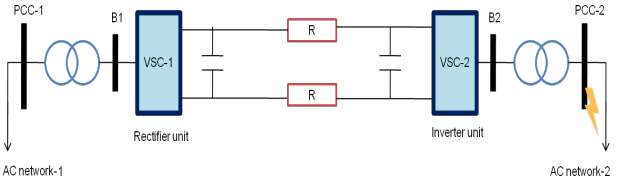

Fig. 13. VSC-HVDC transmission with two-AC networks.

The findings gathered whenever the system is treated towards the 3-phase-to-ground fault at PCC-2 during 140ms are shown in Fig. 14. Like the potential at PCC-2 decreases, the rectifier lowers the real power transmitted via the A.C. network-1 to A.C. network-2. As shown in Fig.14 (a), when every ac network retains its independence, the Voltage at PCC-1 becomes less vulnerable to the A.C. fault on PCC-2. Therefore, as a consequence of retained energy inside the dc link, Fig. 14 (c) indicates a restricted increment in the dc-link Voltage (about 1 percent) and applies restricted voltage stress throughout the valves of the inverter. Fig. 14 (b) displays the real and reactive powers at PCC-1. Ignoring the fact that the Voltage at PCC-2 decreased to zero over the whole fault time, the inverter offers a small current to the fault with a maximum of 1.0pu, as shown in Figs. 14 (d) to (e). This considerably lessens the current stress upon these states of the converter's switches.

Here, we compare our findings with the existing approaches to prove that the proposed approach got a more significant performance capability in the VSC-HVDC network, as depicted in figures (15) and (16). From these figures, we conclude that our proposed work produces smaller fault currents when A.C. and D.C. faults occur. It leads to our proposed work got more excellent capability than the existing techniques in VSC-HVDC transmission.

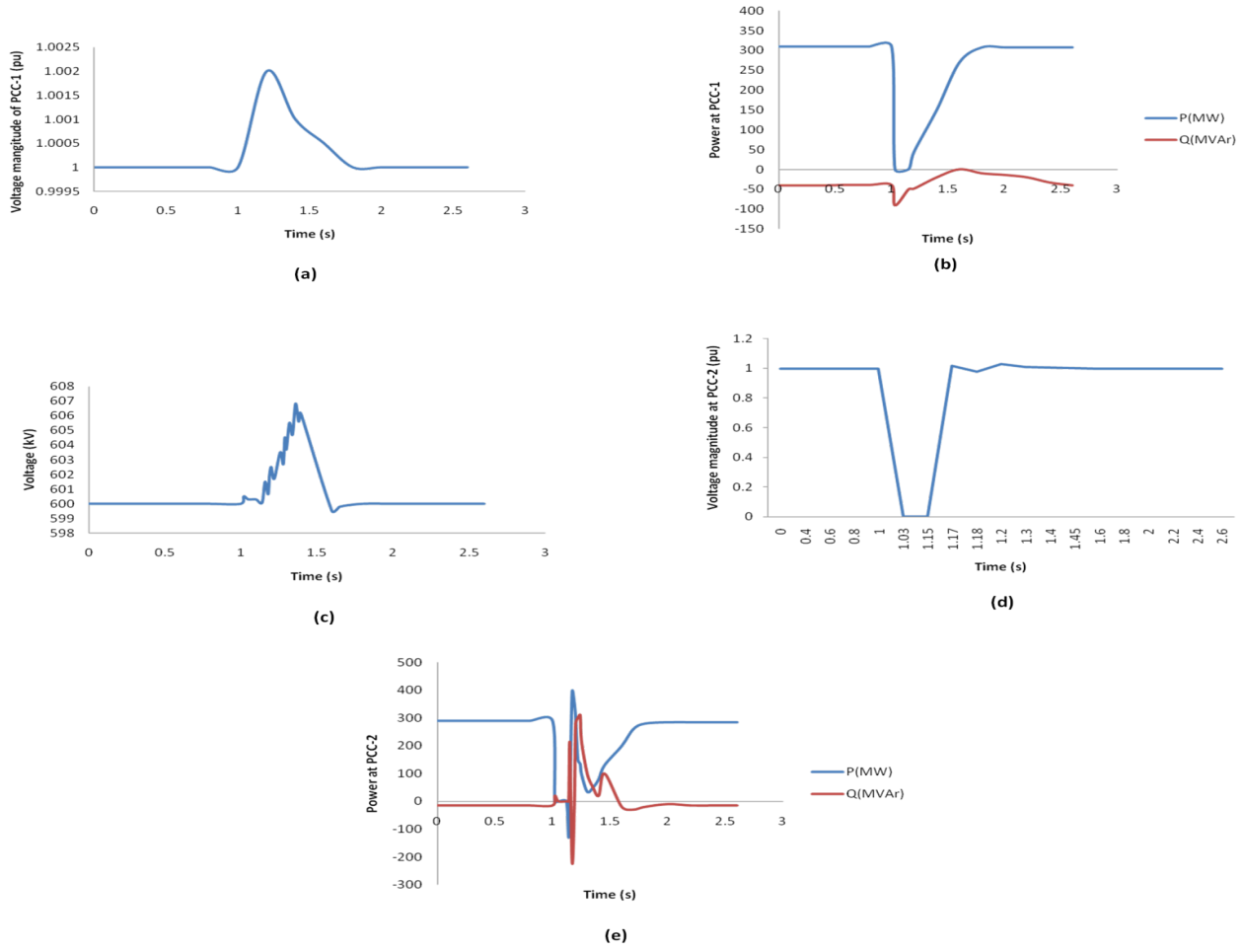

Fig. 14. Voltage and Power waveforms captured at the time of 3-phase-to-ground fault.

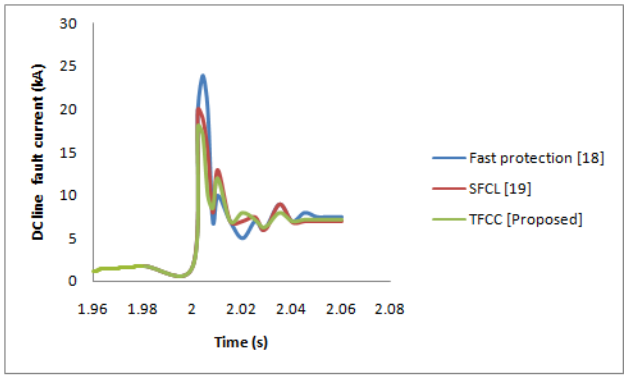

Fig. 15. Comparison of D.C. fault current in proposed and existing approaches.

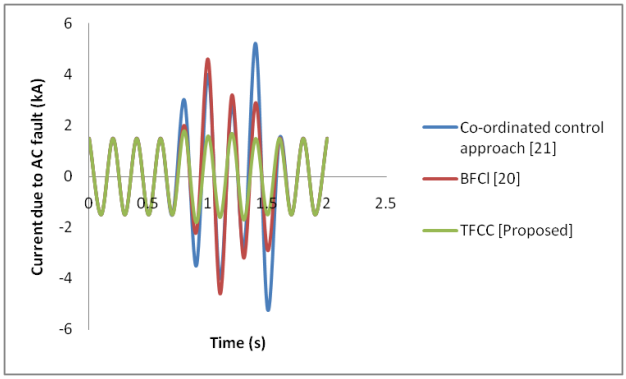

Fig. 16. Comparison of A.C. fault (3-phase-to-ground) current in proposed and existing approaches.

5. Conclusion

As a result of the difficulties involved in design variables, nonlinear dynamics, and disturbances, designing reliable regulators for nonlinear VSC-HVDC transmissions is a significant issue. So, we offer the new TFCC topology based on the inductor and the resistance's current-limiting properties. This research examines the characteristics of the 2-level VSC-HVDC networks during cascading faults (D.C. and A.C. faults) to truly comprehend the network under that kind of fault. The SCCs were protected against quench by the quick D.C. breaker's action. It is done through parametric study, electromagnetic design, and simulations. In calculations and simulations, the impact of design characteristics on the current-limiting impact was shown. Finally, we demonstrated that the proposed approach has superior performance capability to the existing approaches in the VSC-HVDC transmission network.

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