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Power and Area Efficient 9T CNTFET SRAM Bit Cells with Differential Read Scheme for Low Power Applications

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Abstract

Design of VLSI circuits using CMOS technology in the deep submicron range come across many issues like increased leakage power and process variations. Therefore, as an alternative Carbon Nano Tube Field Effect Transistor (CNTFET) is explored for nanoscale range circuits. CNTFET offers high stability, high performance and consumes low power. Low voltage operation and noise tolerant SRAM bit cells have become much essential due to their great usage in low power applications which mainly includes the Bio medical devices. Memory banks with low power are much important since 70% of the die area is surrounded by them. This paper presents two different CNTFET based SRAM bits of 9 transistors using Differential Read Scheme. These designs achieve enhancement in stability and reduction in power with reduced area occupancy. The designs are implemented in Cadence using CNTFET 32nm technology operated at 900mv.

Keywords: CNTFET, SRAM, Biomedical devices, Differential Read Scheme, Stability.

1. Introduction

Since many years, VLSI designers are using MOSFETs as a basic element in the circuits. MOSFET based circuits are used as they drain less power and even cheaper in fabrication [1],[2]. But the demanding essentials of VLSI such as high speed, low power and high chip density can be attained by reducing the transistor size through a well known process called scaling. Due to the scaling down of technology, power consumption becomes worst because of the increased leakage current [3]. This MOS scaling enforces the semiconductor industry to come across various problems such as power dissipation, short channel effect, process variation and leakage current. To conquer the scaling limit, an alternate technology of CNTFET is thus explored as the promising replacement for the future electronics [5]. The CNTFETs are formed by rolling the graphene sheets further forming tubes that are used as the channel in place of silicon. The CNTFETs offers high transconductance, good heat conduction, high carrier mobility and less quantum capacitance. The graphene rolling used and the electrical properties of a CNTFET is given by the chiral vectors(n,m)[6].

Low power applications are of foremost concern in the recent emerging portable System on Chips (SoCs). The Static Random Access Memories(SRAMs) are greatly utilized in the Soc products. As mentioned in [7] by the Int. Tech. Roadmap for Semiconductors (ITRS), most ofa chip area is being occupied by the SRAMs. Therefore, it is necessary to design power efficient, high density, high speed and stable SRAM arrays. Especially, portable applications such as medical implantable devices like pacemakers, hearing aids etc., require less power consuming SRAMs [8] as they are placed inside the human body. In addition to the power consideration, stability of SRAMs is also vital as getting an accurate information of the patient too plays a key role. Area occupancy also has a great contribution as increase in area provides inconvenience to the patients.

Power being the main consideration, the most common step taken to diminish the power consumed is decreasing the supply voltage, as power maintains a quadratic relation with supply voltage [9]. Decreasing the supply voltage, leads the circuit to be operated in the subthreshold region. But, unfortunately the standard 6T cell failed to work reliably in the subthreshold region [10]. Therefore, several configurations are implemented in [11] – [18] to overcome the stability issue of the standard 6Tcell, by making the read and the write paths separated with each other. These configurations either consume more leakage power or use extra transistors or use a single ended read scheme. Leakage power plays a key role as about 40% of the active energy of the SRAM is being consumed by it [19]. Another problem is associated with the usage of a single ended read scheme which is not much potent as the differential one. The single ended read scheme suffers from the bit line swing and the sensing margin during the read operation [20]. To provide an improvement in the read stability, many differential SRAM cells are designed [21] - [23] but with a penalty of large area. This work introduces two designs of the CNTFET based differential SRAM cells with improved stability, reduced leakage power with less area occupancy by reducing the count of the transistors. The paper also introduces the extension of the existing CMOS based SRAM cells by demonstrating them in CNTFET.

The residual part of thebrief is arranged as the following manner. In II-Section, the structures and working principles of the Standard 6T SRAM design and other existing designsusing CNTFET are deliberated. In III-Section, the structure of proposed designs along with their operation is mentioned. Section-IV gives the simulation results and provides comparison of various structures. Finally, section-V winds up with a conclusion.

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2. Standard 6T and other Existing SRAM Designs

Standard CNTFET 6T SRAM bit(C-6T) is the basic bitcell topology of the SRAMs. It has a very simple structure as shown in the Fig.1. The structure comprises of two inverters which are associatedin back to back format, forming a latch capable of holding 1 bit of information. Two pass gate transistors N1 and N2 are used to execute the read & write operations. Its working principle is stated in three different modes: Write, Read and Hold [24].

Write operation deals by enabling the WordLine(WL) such that the two pass gate transistors will be turned ON to get connected with the cell. Now, the information that is intended to move on to the SRAM cell is provided to the two BitLines(BL and BLBar). The enabled WL, thus allows the data of BL and BLBar to be transferred to the cell. The information entered into the cell is now accumulated in the two storage nodes Q and $\overline{Q}$.

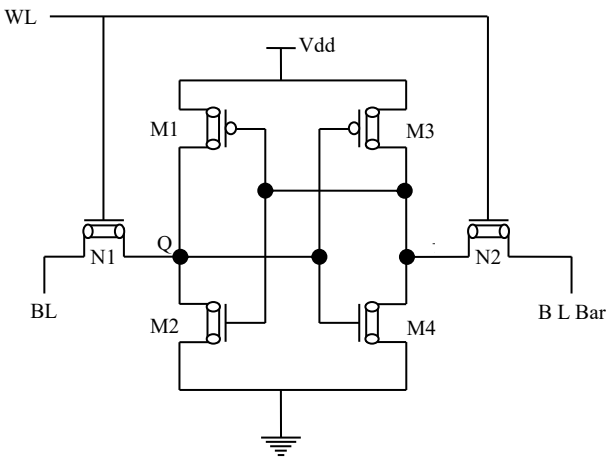

Fig. 1. Standard SRAM Design(C-6T)

Read operation is also executed by enabling WL. Before that, firstly, the two BitLines are precharged to Vdd using a precharge circuit. Now, relying on the informationaccumulated in the storage nodes, any one of the Bitline will be discharged to the ground while the other retains at Vdd. This experiences a small voltage difference among the Bitlines which is then sensed by sense amplifier and gives the final data that is accumulated in the storage nodes of the cell Q &$\overline{Q}$ respectively.

During the Hold state, the WordLine is disabled by turning OFF the pass gate transistors, thereby eliminating the connection of the BitLines from the cell. In such case, the two back to back connected inverters will proceed to reinforce the information

The Standard 6T cell experiences a degraded read stability as it represents a direct contact between the bitlines and the internal storage nodes. Especially, at low voltages it undergoes to a read failure by flipping the data that is accumulated in the cell [25]. To overcome this issue, many designs are developed among which the basic one is the conventional 8T cell [26]. This design defeats the stability issue of the standard 6T design by segregating the read & write ports, enabling them to proceed their operations individually. However, this design, due to its additionally added extra transistors to do so prones to more leakage. Keeping the leakage problem in consideration, some other techniques are developed recently [27]. Such designs involved a stack of transistors which helped in reducing the leakage power [28]. But these techniques employ a single ended strategy which degrades the bitline swing and the sensing margin. In the single ended scheme, the overall bitline leakage greatly bases on the data stored in the cell which may cause data collision between the columns. This scheme also leads to more read delay [29]. Therefore, the researchers preferred the differential sensing scheme which provides much robust results than the single ended one discussed below.

The Fig.2 shows one of the CNTFET based differential read scheme SRAM cell with 10 transistors which is an extension of [30]. This work introduced a new design by placing two access transistors in series. The design also uses decouple read port which makes the storage nodes disconnected with the bitlines through which the read signal noise margin is remarkably improved. Write operation is carried on by activating both the RWL and WWL lines so that the data that is written is transferred to the cell from the bitlines through the access transistors. In read mode, RWL is activated and WWL is deactivated by separating the bitlines with the storage nodes. Now, the information stored in the cell causes the bitlines either to discharge to the ground or to charge to Vdd by depending on the stored data. The voltage difference thus obtained will be sensed by a sense amplifier. In hold state, both the RWL and WWL lines disabled by turning OFF all the four access transistors. This design, making use of stacked bitline leakage paths of the transistors, reduces the leakage power. But utilization of 10 transistors makes it to occupy more area. This work also faces the write ability problem as it uses series of access transistors.

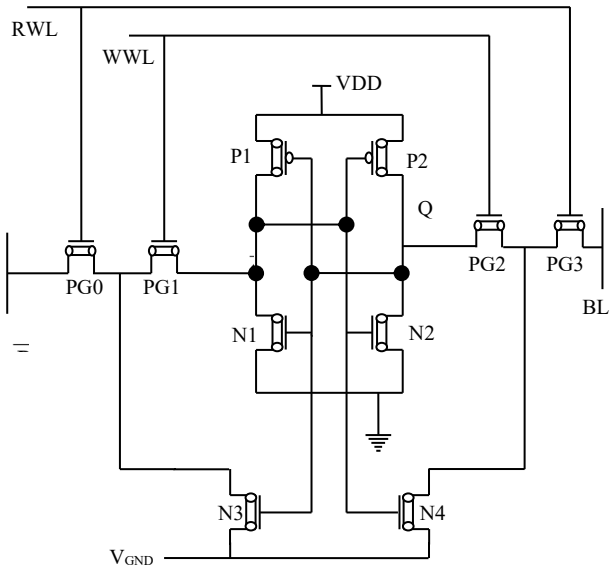

Fig. 2. Diff. 10T SRAM Cell(E1-10T).

Another technique of CNTFET based differential read scheme of a Zigzag 8T SRAM cell which is an extension of [31] is shown in Fig.3. This design with its similarity with the standard 6T one adds a 2T decoupled read port using a differential scheme. The two added decoupled transistors N3 and N4 are used to perform the read operation making use of separate Read BitLines RBL and $\overline{RBL}$. Thus, the storage nodes are totally disconnected from read bitlines through which the static noise margin is improved. This design thus resolves the issue of the read disturbance. During write mode, the Write WordLine(WWL) is enabled and the operation takes place identical to the standard 6T one. Read operation is done in a different passion by giving a low pulse to the Read

WordLine(RWL). Now, the value held in the storage nodes Q &$\overline{Q}$makes one of the RBLs to discharge to ground and the other to be held at Vdd. Voltage difference thus developed will be sensed by a differential sense amplifier. For Hold operation, the WWL is disabled and the RWL is maintained at Vdd.

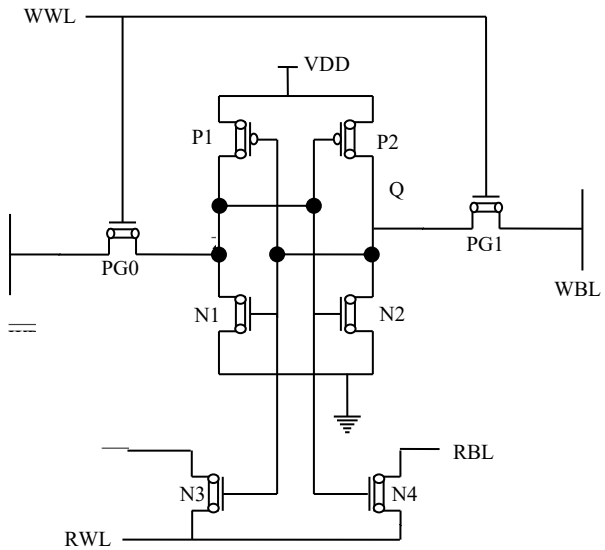

Fig. 3. Diff. 8T SRAM Cell(E2-8T).

This design, through its differential scheme improves the Read Noise Margin than the standard 6T design, achieves faster read process and employs small swing. But, at the same moment is prone to more read power consumption as it makes use of additional two bitlines for performing the read operation. This brief presents twoCNTFET based 9T SRAM bit cells with fully differential read scheme as explained in the below section.

3. Proposed Designs

The schematics of proposed designs using CNTFET isrepresented in the Fig.4. Both of the structures making use of 9 transistors enables to reduce the area occupancy. This is achieved by considering the write operation using only a single bitline which also further reduces the power consumption. Each of the design follows the basic operating principle of the standard 6T cell during the write mode but with a single bitline(BL). The operating principle during read mode varies in each design improving the stability and reducing the read power and leakage power consumption. Fig.4(a) shows the first work of paper(P1-9T) using CNTFET. The cell comprises of 9 transistors with four extra transistors (N4, N5, N6 & N7) and one Read Line(RL) to carry on the read operation. During write process, the Word Line(WL) is set enabled and RL is disabled. Due to the enabled WL, the access transistor N3 is turned ON to pass on the data from the bitline BL to the core cell. For writing '1' to the cell, BL is loaded with '1' and thereby through N3 transistor '1' is accumulated in the node Q. Thus the desired data is written successfully.

During the Read process, RL is enabled & WL is disabled by isolating the bitlines with the storage nodes such that the read noise margin is improved. Now, relying on the data present in the storage nodes, the read operation is performed. For instance, if Q is stored with '1' and $\overline{Q}$with '0', then $\overline{BL}$discharges through N5 & N7 while BL is held at Vdd. Alternatively, if Q is stored with '0' and $\overline{Q}$ with '1', then BL discharges through the path developed by N4 & N6 and $\overline{BL}$ held at Vdd. The voltage difference thus occurred between BL & $\overline{BL}$will be given to the sense amplifier (not shown here) that gives the stored data. During hold mode, both the WL & RLs are disabled making the access transistor to turn OFF. This design helps in reducing the leakage power since it uses stack of transistors at the read path.

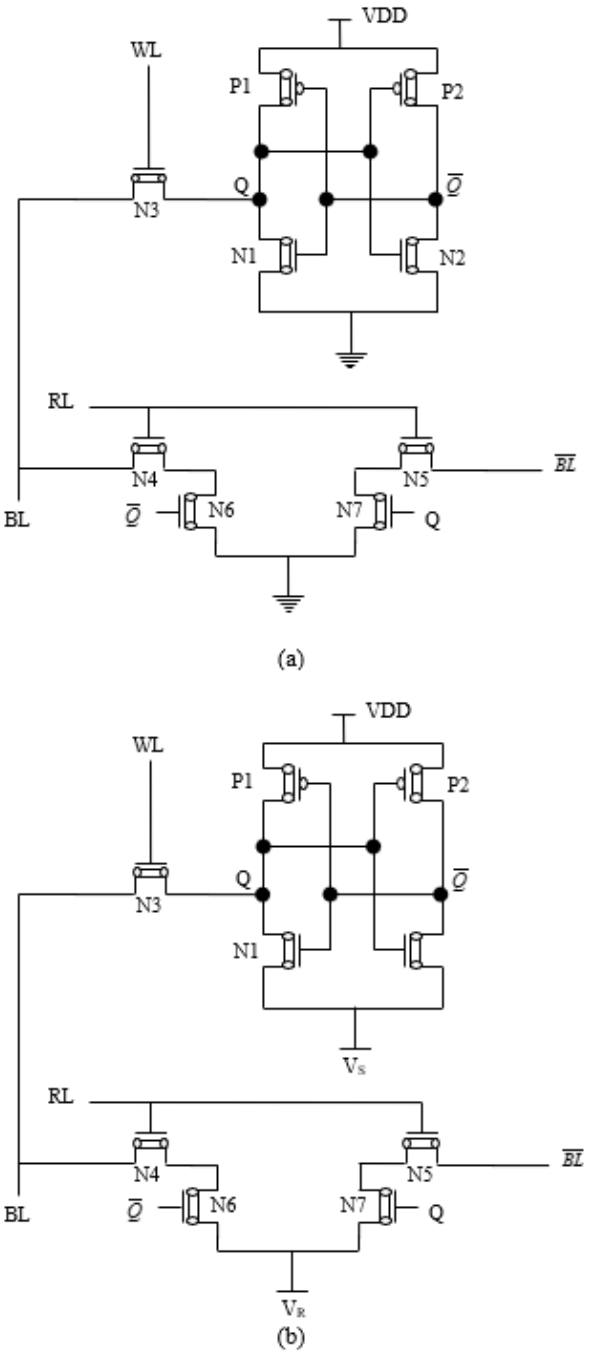

Fig. 4. (a). P1-9T SRAM Cell, (b). P2-9T SRAM Cell.

Since Leakage power is main consideration in order to diminish the overall power consumption of the die, in this brief one more design is proposed based on CNTFET. This is achieved by inserting Row-based signals V_S and V_R at the read and write path of the cell as represented inFig.4(b). Thereby, this design further minimizes the power consumption to some more extent. Write process is similar to that of P1-9T as mentioned above with a slight difference of maintaining the

added row based V_S and V_R to GND and Vdd respectively. The maintained V_S makes the data stored retain in the core cell. Read process is carried on by maintaining both V_S and V_R to GND, enabling RL and disabling WL by disconnecting the bitlines and the storage nodes through which the read noise margin can be improved. V_S is maintained to GND in order to retain the data in the core cell. Read operation is commensed by initially precharging BL &$\overline{BL}$s and then enabling the RL. Now, relying on the storage nodes data Q and $\overline{Q}$, the bitlines will charge or discharge accordingly. If Q stores '1' and $\overline{Q}$ stores '0', $\overline{BL}$ discharges through N5,N7 & V_R and BL held at Vdd. Furthermore, if Q stores '0' and $\overline{Q}$ stores '1', BL discharges through N4,N6 & V_R and $\overline{BL}$ held at Vdd. The potential difference thus obtained is sensed by the sense amplifier (not shown here) which gives the appropriate data that is stored in the cell. During the Standby mode, RL and WL are disabled. V_S and V_R are maintained at Vdd such that to reduce the bitline leakage. Since they are used as Row-based i.e making use of them for the cells of one entire row instead of considering for each and every cell, the area occupancy can be reduced.

4. Simulation Results and Discussion

The Timing diagram during the read process of proposed design is represented in the Fig.5. The CNTFET 32nm technology has been used for Cadence simulator to implement all the simulations operated at 900mV.

Comparison of the proposed versions is carried for the read and write operations,as the design is concentratedto perform the read process using the differential read scheme to achieve better read noise margin and to perform the write operation using single bitline to achieve area and power reduction. Basically, the SRAM's performance is mainly based on the power consumption, stability, delay & area occupancy. In this section, comparison of different SRAM designsalong with the proposed versions using CNTFET is done for various parameters as mentioned in Table.1. The leakage power is calculated for both the cases i,e, the cell stored with '0' and the cell stored with "1'.

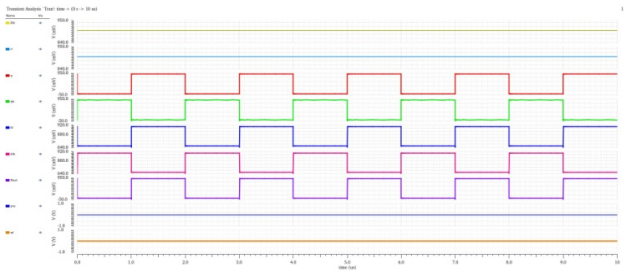

Fig. 5. Timing diagram for Read operation of proposed design

Since the proposed versions use only 9 transistors to carry on the working operation, they can reduce the area occupancy of the chip when compared to many other designs which make use of 10 or even more transistors. As power is the main metric of SRAM design, it is necessary to make sure that the power consumed by the cell should be less. The proposed versions, making use of a single bitline to perform the write operation, thus achieves good power reduction when compared to C-6T, E1-10T & E2-8T as shown in Fig.6. This is so because as C-6T, E1-10T & E2-8T use two complementary bitlines to write the data into the cell the charging and discharging of two bitlines consume more power. Fig.7 gives the comparison of Read power. The two proposed designs consumes less Read power compared to E2-8T. It is because E2-8T uses additional bitlines to perform the read operation. Since almost all the designs that are considered and proposed, uses stack of transistors at the read path, the leakage power will be homogeneous. But at the same time, the inclusion of Row-based V_S and V_R to P2-9T suppresses the BL leakage to further extent compared to the other designs and becomes equal to that of the conventional C-6T design as represented in Fig.10.

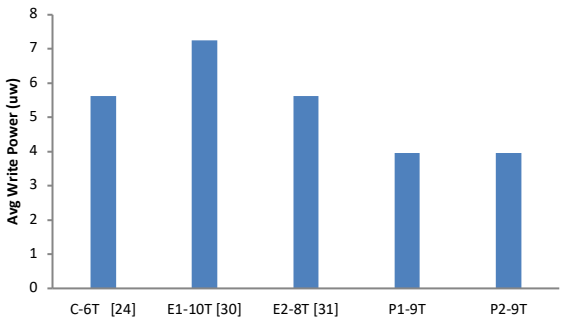

Fig. 6. Write power comparison.

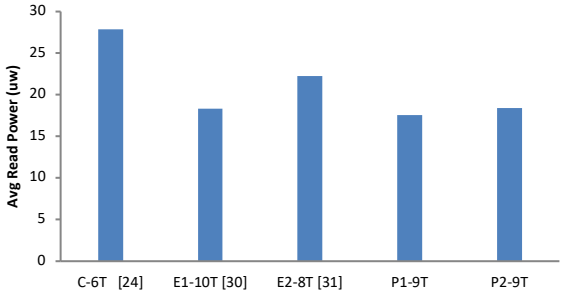

Fig. 7. Read power comparison.

Table 1. Parameters Comparison

	C-6T [24]	E1-10T [30]	E2-8T [31]	P1-9T	P2-9T
TechnologyCNTFET (nm)	32	32	32	32	32
Supply Voltage (mV)	900	900	900	900	900
Write Power (uW)	5.62	7.25	5.62	3.96	3.96
Read Power (uW)	27.9	18.35	22.23	17.56	18.43
Read SNM (mV)	150	325	315	320	325
Leakage Power (pW)					
0	67.18	74.36	81.54	74.43	66.84
1	66.36	74.07	81.13	74.24	66.15

Fig.8 and Fig.9 gives the Write and Read power comparison of the existing and the proposed cells at different voltages respectively.

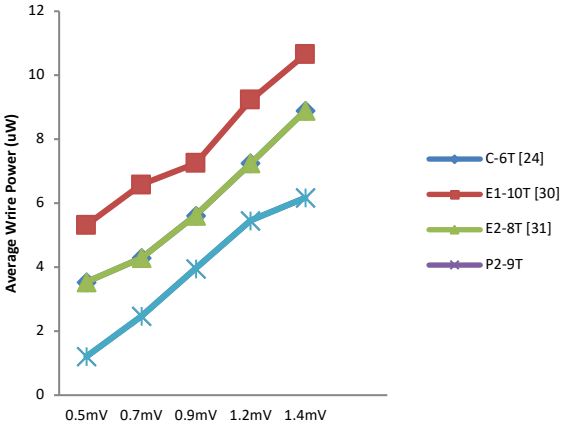

Fig. 8. Write power comparison at different voltages.

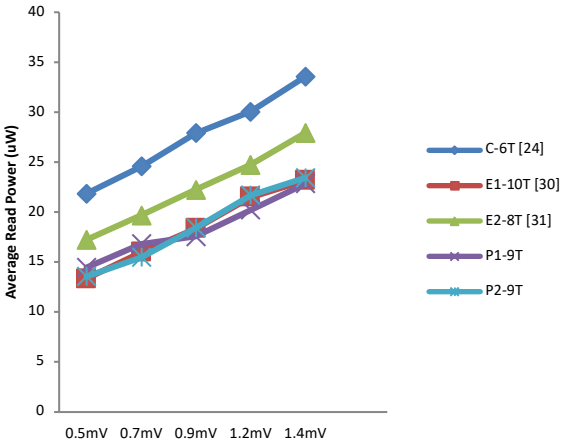

Fig. 9. Read power comparison at different voltages.

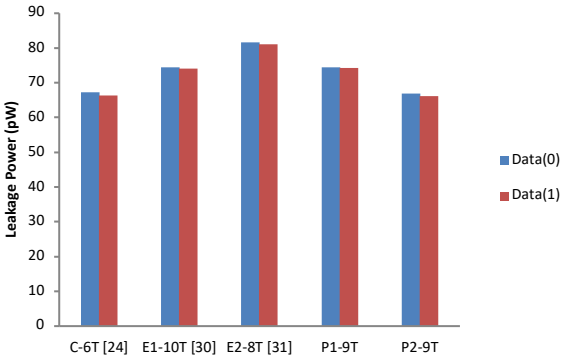

Fig. 10. Leakage power comparison.

Read noise margin is a criterion to study the stability of the SRAM cell during read mechanism. It is given as the min voltage noise required to change the cell's state. The proposed versions, as are based on differential read scheme, gives better stability when compared with the single ended techniques. The proposed versions produce better improvement in RNM compared to C-6T since the read & write operations are isolated and also produces about similar results compared to other two existing techniques as represented in the Fig.11.

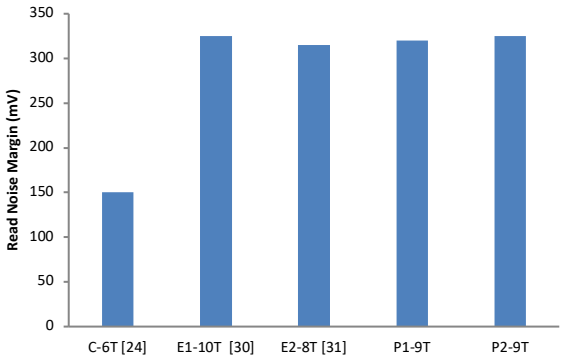

Fig. 11. RNM comparison.

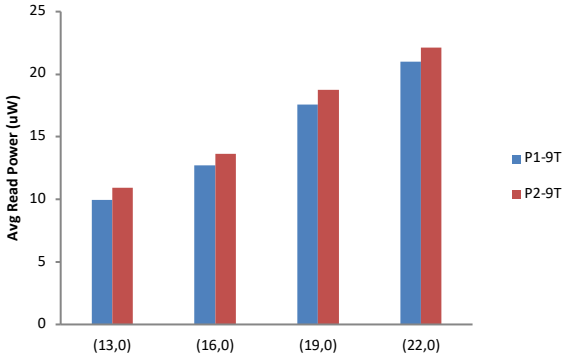

Fig. 12. Read Power comparison of the proposed cells at different chiral values.

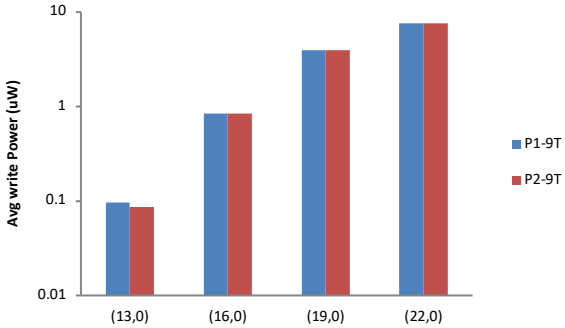

Fig. 13. Write Power comparison of the proposed cells at different chiral values.

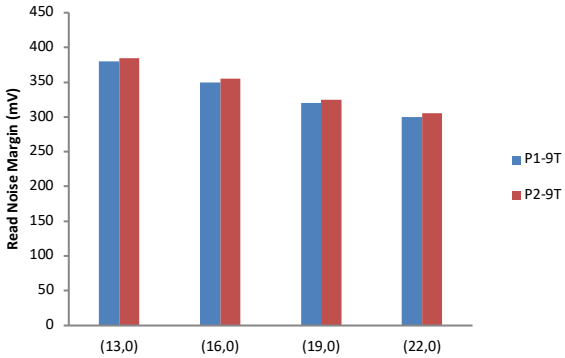

Fig. 14. Read Noise Margin comparison of the proposed cells at different chiral values.

Fig.12 to Fig.16 represents the Read power, Write power, Read noise margin, Leakage power when the stored data is '1'

and the Leakage power when the stored data is '0' at different chirality values. It is clear that better Power consumption and good Noise Margin can be achieved as the chirality values goes down.

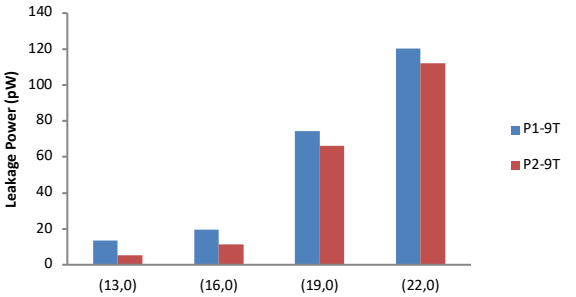

Fig. 15. Leakage Power comparison of the proposed cells (With stored Data-1)) at different chiral values.

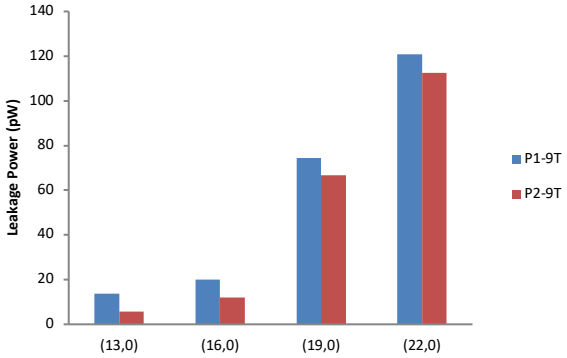

Fig. 16. Leakage Power comparison of the proposed cells(With stored Data-0)) at different chiral values.

5. Conclusion

Two versions of proposed designs using CNTFET are presented in this brief to enhance the read stability, while reducing the writeand readpower compared to C-6T, E1-10T & E2-8T designs. The brief proposes a differential read scheme using to carry out the read operation to enhance the read disturbance. Usage of single bitline and row based signals reduces the area overhead. Analysis is performed on impact of the parameters such as read power, Write power, Leakage power and stability. Better improvements are observed when compared to the rest of the designs considered in this paper.

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