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Performance Analysis of GAA MOSFET for Lower Technology Nodes.

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Abstract

With the continuous down scaling of transistor size in order to improve the packing density, pushing the transistor design into different level. Starting from planar structure to complex 3-D nanoelectronics devices, the device performance changes drastically as the miniaturization of device dimension occurs to attain current need of the semiconductor industry. In this work the performance analysis of different Figure of merits (FOMs) are studied extensively for lower technology nodes. The transfer and output characteristics are provided with different gate and drain bias to study the sub-threshold and short channel effects. Apart from that some simulator generated structures are provided to visualize the surface potential and electric field completely. The superiority of Gate All Around (GAA) MOSFET over other conventional MOSFET in Nano scale paving a path for next generation transistor scaling.

Keyword: GAA, MOSFET, Nano, Scaling, Sub-threshold

1. Introduction

With the creation of the first transistor in 1947, the whole semiconductor industry witnessed an immense revolution and the vision of the semiconductor industries changed entirely. As the transistors size reduced drastically, the Moore's prediction towards transistor scaling started to diminish. Apart from transistor scaling, researchers start to find new techniques to add more number of transistors in a single chip. By introducing scaling techniques to the gate is not the ultimate solution to improve the device performance with improved packing density and low cost. Continuous scaling of device size with reduced channel length creates some unwanted effects like the channel length modulation, short channel effect, threshold voltage roll-off, punch through effect, parasitic capacitance increment and drain induced barrier lowering (DIBL). At the same time reduced gate oxide thickness leads to severe quantum mechanical effects and hence resulting more leakage current. As the traditional planar MOSFET design slowed down due to scaling problems. New material or gate engineering was necessary in order to match the current requirement of semiconductor industries. By keeping Moore's law in mind, many new devices have been proposed and the performances were extensively investigated. This era is called more than Moore or MtM development era. Instead of believing only on device scaling, different engineering techniques were introduced to fulfill the semiconductor industry requirement [1-5]. Power dissipation is one of the key factors that is responsible for supporting Moore's law in lower technology node. Therefore, low voltage with low power device and circuits are necessary for state of the art device design. The scaling of device channel length reached at 5nm in 2019, which was nearly 180nm in 2010. Different advancement in VLSI occurred during the year 2015-2019 in order to develop advanced circuits to meet the current needs [6-10]. At the same time different engineering techniques were proposed by different researchers to continue Moore's law in near future.

Some multigate structure using SOI technology has been proposed to replace the conventional MOSFET [11-13]. Cylindrical gate all around (CGAA) structure has the capability to enable the scaling further without deteriorating the device performance. It has beaten all its competitors irrespective of the type and size of the device geometry and became a promising device for next generation nanoscale technology CMOS devices [12-18]. In this chapter, some important performance metrics such as drain current (ID), off state current (Ioff), transconductance (gm) and threshold voltage are extensively investigated with the variations of gate length (Lg), metal gate work-function (Φm) and silicon thickness (tsi) in details.

2. Device Design and Simulation

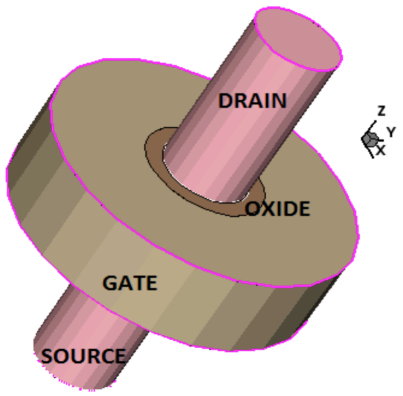

Fig. 1. 3-D Pictorial view of the proposed model

Figure 1, shows the pictorial depiction of the proposed model

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in 3-D view. With an extended source and drain terminal, the proposed device has a gate length of 20 nm with gate metal work-function as 4.7eV. The gate metal thickness is kept around 9nm. The gate oxide thickness (t_{OX}) is kept 2nm. The proposed device is a multigate MOSFET structure. As the gate is wrapping the channel from all around, so it is named as gate all around (GAA) MOSFET. The details about device dimensions are given in table 1.

The structure editor Sentaurus Structure Editor for 2D and 3D device structures [20]. It had 3 operational modes: They are 2D structure editing, 3D structure editing, and 3D process emulation. 2D and 3D device models are created geometrically from the graphical user interface (GUI), using 2D or 3D structures, like the rectangles, polygons, cuboids, cylinders, and the spheres. The command line window features in GUI of Sentaurus Structure Editor, in this window the Sentaurus Structure Editor prints the script commands as per the GUI operations. The device includes different physics based model for micrometer technology as well as nanometer technology. Apart from drift diffusion models it is also includes quantum based model to investigate the nano scale devices extensively. Apart from these it also includes thermodynamic and hydro dynamic models also.

Table 1. Device dimensions and Specifications

Device Parameters	***Device dimension and specification***
Oxide (SiO_2 thickness (t_{ox})	2nm
Channel (Silicon) length (L)	10-50nm
Cylinder pillar diameter (t_{si})	10nm
Control Gate metal work function (M_1)	4.6ev(Molybdenum)

3. Math

The analytical model of the cylindrical gate all around GAA can be developed by using different boundary conditions in the cylindrical coordinate. Those boundaries include the source-channel and drain-channel, where the potential is due to the built in potential and drain voltage. The potential through the silicon film is different at different boundaries. The potential distribution $\varphi(r,z)$ on the silicon filmalong the z-direction is governed by Poisson's equation in the cylindrical coordinate [15]. The equation is a 2-D equation as it depends on two variables i.e 'r' and 'z'.

$$\frac{\partial^2\varphi(r,z)}{\partial z^2}+\frac{1}{r}\frac{\partial^2\varphi(r,z)}{\partial z^2}+\frac{\partial^2\varphi(r,z)}{\partial z^2}=\frac{qN_a}{\epsilon_{si}} \quad (1)$$

surface potential distribution in the channel regions can be expressed as a parabolic function in the form

$$\varphi(r,z)=C_0(z)+C_1(z)r+C_2(z)r^2 \quad (2)$$

Different boundary conditions associated with a cylindrical structure are given by the following equations, which will determine the arbitrary coefficients$C_0(z), C_1(z)$ and$C_2(z)$.

The centre potential is a function of 'z' where $r=0$.

$$\varphi_c(r=0,z)=\varphi_c(z)=C_0(z) \quad (3)$$

The electric field in the center of silicon pillar is zero due to radial symmetry.

$$\frac{\partial\varphi(r,z)}{\partial r}|r=0=C_1(z) \quad (4)$$

The electric field near the Si/SiO_2 interface can be represented by

$$\frac{\partial\varphi_s(r,z)}{\partial r}|r=\frac{t_{si}}{2}=\frac{2\epsilon_{ox}}{\epsilon_{si}}\frac{\varphi_{GS}-\varphi(r,z)}{t_{si}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}=t_{si}C_2(z)$$

$$=\frac{\epsilon_{ox}}{\epsilon_{si}}\frac{(V_{GS}-V_{FB}-\varphi_s(z))}{t'_{ox}}=t_{si}C_2(z) \quad (5)$$

4. Results and Discussions

The simulation based model for the proposed device in different technology nodes were investigated properly by taking different channel length. The device parameters and physics based equations were included in the SDEVICE section to match the exact behavior of the simulation results. Formulation of surface potential for both the models were carried out to calculate the drain current and other figure of merits (FOMs). When a small voltage is applied to the gate, a potential is developed at the oxide-channel interface that controls the charge carriers. In case of GAA, except at source-channel and drain-channel boundary the potential is almost same. Figure 2. illustrates the surface potential profile of both the models w.r.t channel length for a small gate bias of 0.1 V.

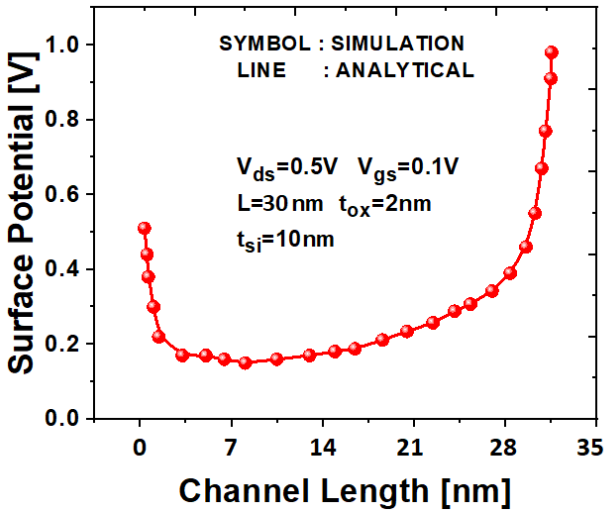

Fig. 2. Electrostatic potential of the proposed model for 30nm channel length

The electric field associated with the device can be extracted by taking derivative of electrostatic potential. The electric field associated with the device can be experienced from the following figure 3. From the figure, the electric field distribution throughout the channel as well as metallic body can be easily identified. Also it can be noticed that the electric field towards the source is comparatively more than towards the drain. Apart from that it can be noticed that the electric field is illuminating from the channel and spreading through the gate metal uniformly as shown in figure.

Figure 4. is showing the transfer characteristic of the proposed model with a gate length of 10nm and a drain bias varied from 0.1V-1.0V. The transfer characteristic thus obtained shows almost equal behavior, if the drain bias is

0.5V and 1.0V. But with lower drain bias (0.1V), the drain current is small compared to the others.

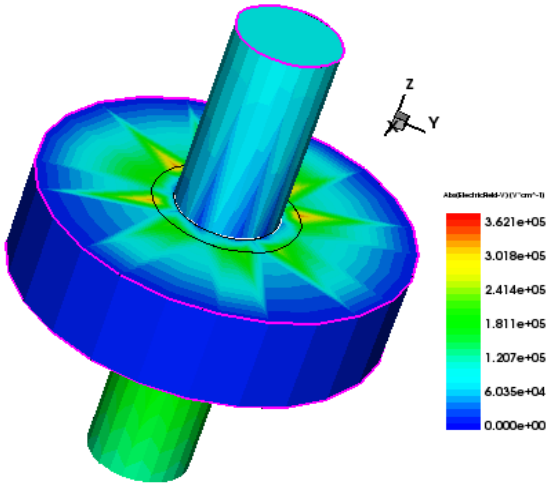

Fig. 3. Electric field distribution of the proposed model

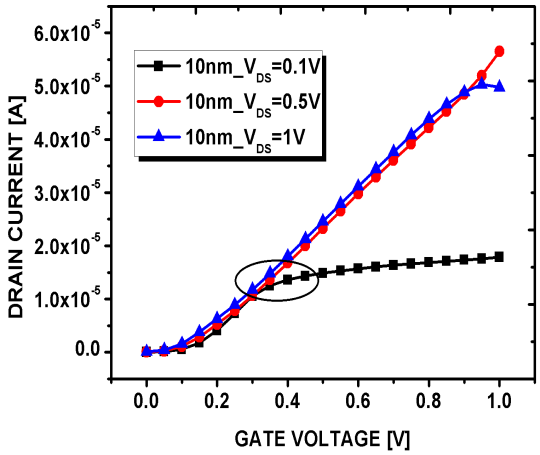

Fig. 4. Drain current vs Gate voltage of the proposed model with different drain voltage.

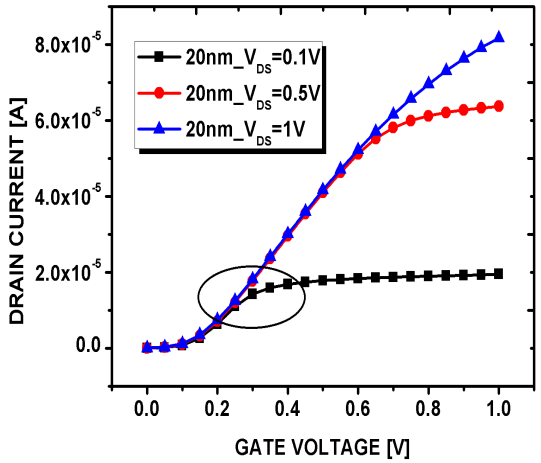

Fig. 5. Drain current vs Gate voltage of the proposed model for 20nm gate length with different drain voltage

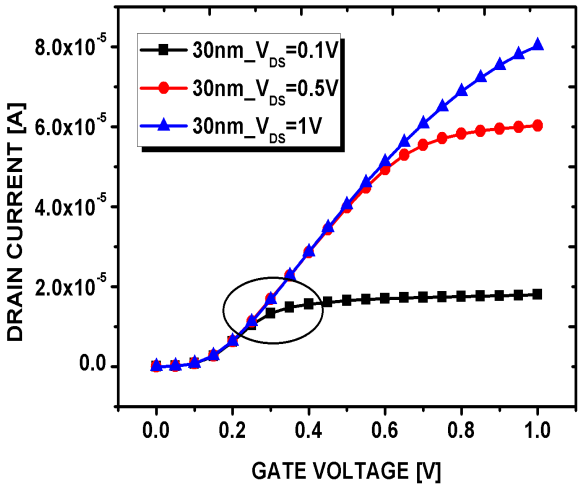

Fig. 6. Drain current vs Gate voltage of the proposed model for 30nm gate length with different drain voltage.

Similar transfer characteristics is carried out for the GAA MOSFET at 20nm gate length for a drain voltage of 0.1V,0.5V and 1.0V. The results thus obtained are different compared to the previous one (Fig. 5). In this case similar to the previous one, the drain current is very low for a drain voltage of 0.1V. But for 0.5V and 1.0V drain bias, the drain currents are not equal as it was earlier.

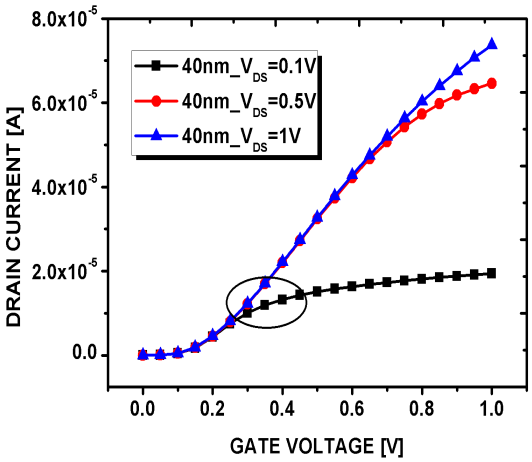

Fig. 7. Drain current vs Gate voltage of the proposed model for 40nm gate length with different drain voltage.

Similar behavior is obtained for 30nm and 40nm gate length for the drain voltage of 0.1V. However, for 0.5V and 1.0V, the behavior is little bit similar to the lower technology node i.e 10nm as shown in figure 7 and figure 5 respectively. The on current and off current and for all the nodes are calculated and shown in table 2 below.

Table 2. On current and Off current values of the proposed model

Gate length	GAA (Vgs=1V, Vds=0.5V)	
10nm	I_{On}=6.68μA	I_{Off}=2.44pA
20nm	I_{On}=7.67μA	I_{Off}=0.114pA
30nm	I_{On}=8.4μA	I_{Off}=0.0386pA
40nm	I_{On}=8.16μA	I_{Off}=0.0246pA

The result analysis is further carried out for different gate length and the corresponding FOMs were illustrated in figure

8,9, and 10 respectively. Apart from that the silicon channel thickness also varied from 5nm-30 nm and the corresponding threshold voltage changes also observed in figure 11.

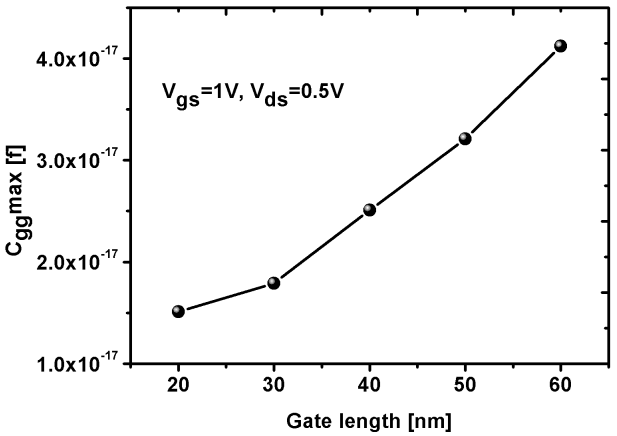

Fig. 8. Total gate capacitance (C_{gg}) vs different gate length (L_g) for the proposed model.

Figure 8 shows the total gate capacitance variation for different gate length starting from 20nm to 60 nm. As the gate length increases, the total gate capacitance increases due to more metal and oxide. At the same time the variation in cutoff frequency with different gate length is illustrated in figure 10. From the figure, it can be easily observed that the variation of cutoff frequency and total gate capacitance with respect to different gate length are reciprocal to each other. The increase in cutoff frequency in lower technology nodes is due to improved drain current and higher transconductance. As the cutoff frequency depends on both transconductance and total gate capacitance, so increase in transconductance with decrease in total gate capacitance results higher cutoff frequency.

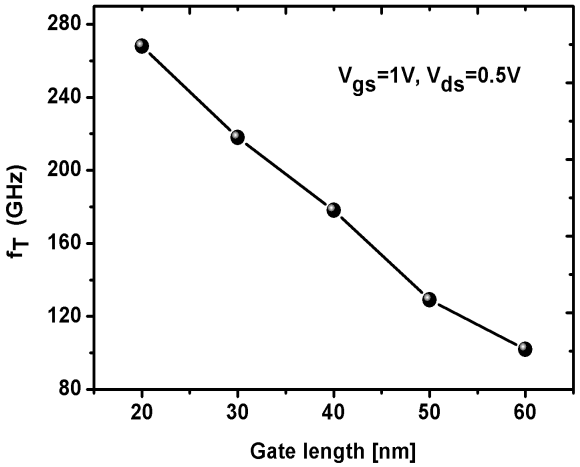

Fig. 9. Cutoff frequency (f_T) vs different gate length (L_g) for the proposed model.

The variation in threshold voltage for different gate length is illustrated in figure 10. From the figure it can be observed that with increase in gate length, the threshold voltage increases. At the same time the behavior of the threshold voltage variation with different channel thickness is observed. With the increase in channel thickness, the threshold voltage reduces drastically as shown in figure 11.

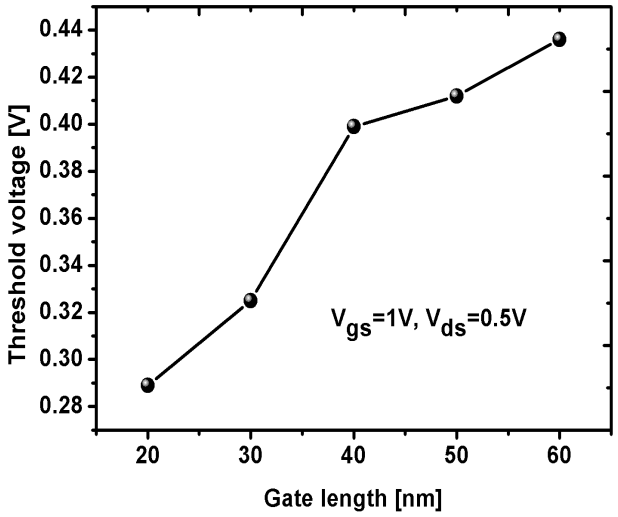

Fig. 10. Threshold voltage (V_{th}) vs different gate length for the proposed model.

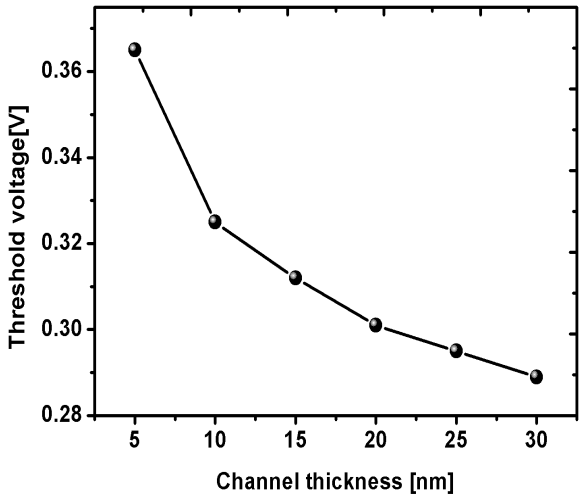

Fig. 11. Threshold voltage (V_{th}) vs different channel thickness (t_{si}) for the proposed model.

5. Conclusion

In this work we have developed a cylindrical GAA MOSFET. The FOMs like On current and Off current are studied extensively with different technology nodes. Apart from this, the gate length of the proposed device is scaled down to 10nm in order to examine the quantum potential behavior that will affect the On current and Off current. And we concluded that at lower technology node the FOMs are getting affected by quantum effects. Apart from these the electric field distribution inside the proposed device is also studied extensively. An analytical surface potential based model is developed to validate the simulation result and will be thoroughly investigate in our future work.

References

1. C. P. Auth and J. D. Plummer, "Scaling theory for Cylindrical, Fully depleted, Surrounding Gate MOSFETs", IEEE Electron Device Lett., vol. 18, (1997) 74.
2. K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs," IEEE Tran. on Electron Devices, vol. 40, (1993) 2326.
3. A.Chaudhry and M. J. Kumar, "Controlling short-channel effects in deep submicron SOI MOSFETs for improved reliability: A review," IEEE Trans. Device Mater. Rel., vol. 4, (2004) 99.
4. A.A Orouji,M.Jagadesh Kumar, "A new symmetrical double gate nano scale MOSFET with asymmetrical side gates for electrically induced source/drain",Micro electron.Eng., vol. 83, (2006) 409.
5. T.K. Chiang, "A scaling theory for fully-depleted, surrounding-gate MOSFET's: including effective conducting path effect", Microelectronic Engineering**.** vol. 77, (2005) 175.
6. M. Mudavath., K. Hari Kishore, Design of CMOS RF front-end of low noise amplifier for LTE system applications, Asian Journal of Information Technology, Vol: 15(2016), 4040.
7. V..Kumar ., S. Shameem S., G.V. Ganesh, Optimum resolution of phase frequency detector by CMOS technology for PLL, International Journal of Engineering and Technology, Vol: 7(2016), 2240.
8. S.Rooban, K. Lakshmi Swathi, Ch.Monica, B.Shivaramakrishna., An Odd Parity Genertor Design Using NanoElectronics, International Journal of Engineering and Advanced Technology, Vol:8(2019), 597.
9. K. .Hari Kishore., D. Koteswara Rao, G. Manvith., K. Biswanth , P. Alekhya, Area, power and delay efficient 2-bit magnitude comparator using modified gdi technique in tanner 180nm technology, International Journal of Engineering and Technology(UAE) ,Vol: 7(2018) ,90.
10. P. Ramakrishna , K. Hari Kishore ,Design of low power 10GS/s 6-Bit DAC using CMOS technology, Journal of Advanced Research in Dynamical and Control Systems ,Vol: 10(2018),878
11. S. Hyun Oh, D. Monroe, J. M. Hergenrother,"Analytic description of short channel effects in fully depleted Double gate and cylindrical surrounding gate MOSFET",IEEE Electron Device Letters, vol. 21(2000) 445.
12. D. Jimenez et al.,"Continuous Analytic I-V Model for Surrounding gate MOSFETs", IEEE Electron Device Letters,vol.25(2004)571.
13. T.K. Chiang,"A New Two dimensional Analytical Model for Threshold Voltage in Undoped Surrounding gate MOSFETs", Solid-State and Integrated Circuit Technology, 2006(1234).
14. L. Zhang,J. He, J. Zhang, J. Feng,"A continuous yet Explicit In 2006,a carrier based core model for the long channel undoped cylindrical surrounding gate MOSFETs",NSTI-Nanotech, vol 3,(2008) 590.
15. B. Jena, S. Dash, K.P Pradhan, S.K Mohapatra, P.K Sahu, G.P Mishra, "Performance analysis of undoped cylindrical gate all around (GAA) MOSFET at subthreshold regime", Advances IN Natural Sciences: Nanoscience and Nanotechnology, vol 6 (2015), 035010.
16. B. Jena, S. Dash, G.P Mishra, "Effect of underlap length variation on DC/RF performance of dual material cylindrical MOS", International Journal of Numerical Modelling: Electronic networks, Devices and Fields, vol 30 (2016),e2175.
17. L. Zhang,C. Ma, J. He, X. Lin, M. Chan ,"Analytical solution of subthreshold channel potential of gate underlap cylindricalgate-all-aroundMOSFET",Solid-StateElectronics, vol54 (2010) 806.
18. B.Jena,S.Dash,S.Routray,G.PMishra,"Inner-Gate-Engineered GAA MOSFET to Enhance the Electrostatic Integrity" NANO: Brief Reports and Reviews, vol 14(2019), 1950128.
19. http://www.itrs.net/reports.html
20. Sentaurus TCAD user guide.