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Study of HDL Optimization Approach for SDR Transceiver Based QAM Scheme

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Abstract

The Hardware Description Language (HDL) optimization approach to use for Software Defined Radio (SDR) transceiver under Quadrature Amplitude Modulation (QAM) scheme is present in this paper. The HDL code plays vital roles in implementation of current and future communication system. The QAM modulator is digitally established in HDL code or Verilog language which combined utilization Register Transfer Level (RTL) complier. The top level design of timing and frequency recovery has used to recover the received bits and decreases the error which will happen in received data. Automatic gain control circuit has used to provide efficient frequency offset estimation and control the system gain as possible. The optimized HDL completion flow chart is planned based on System Generator requirements to generate the required file for Field-Programmable Gate Array (FPGA) realization. The fundamental of SDR is a most accepted prototype proposal for wireless system due to high elasticity. This work show the methods of top level structure of SDR platform depend on QAM scheme. Overall communication system include transmitter, receiver and channel is designing and running in MATLAB to show the system behavior and performance of suggested SDR structure. For hardware competence, the synchronization algorithms of timing recovery, carrier frequency and phase offset were optimized. The results show efficient transmitter and receiver performance with low error in data transfer which will support the future wireless systems.

Keywords: HDL Optimization, SDR Transceiver, QAM Scheme

1. Introduction

The idea of software defined radio (SDR) is presented first time early 1991 in Paris international conference by [1]. The development of physical layer under SDR technology pretenses multitude of challenges due to radio frequency mixed signal in first time research experiments. These challenges comprise the difficulty in collaborating of system integration and evaluation of baseband algorithms with the scenario of radio frequency filed [2]. The evaluation of multipath fading effect and radio frequency interference is the most problems popular in that time. The researcher was seeing that the bang of hardware radio as a mean of communication include audio and visual data over vast distance. The most radio is hardware define without software controlling with short life and designed to be changed and useless [3]. After that, the analogue radio was changed to digital radio in many applications and programmable hardware radio become more interested in digital system. Currently, many commercial communication systems facing difficulty because of limitation in evaluation of link protocol such as mobile generations [4]. Incompatibility of wireless technology such as global roaming presence in handset of subscriber is appearing. All the above mentioned problem could be solve by SDR technology which is incorporate of both hardware and software with reprogrammable functions in term of FPGA generation [5]. In the same technology, one could build a structure of modulation, demodulation and coding section in wireless communication systems sections as close as possible to the antenna. By using software controlling technology, the gap between link layers could be solved to achieve quick solution of many problems such as global roaming by design generic platform able to switch the model functionality as an open system with all services. The requirement of SDR architecture requires A/D and D/A conversion section to be close with antenna as possible to enable directly the RF or IF sampling rate process. The practical and robust SDR design requires also high dynamic range, amplifiers and PLL device. The SDR enable product in much industry led to change from analogue equipment from single chip to programmable wide band module with high performance.

The functional block diagrams of SDR technology showing in Figure 1 illustrate the duty of each part in the system [6]. The analogue front end includes filtering and conversion process and the digital front end consist of sample rate conversion and digital processing. The baseband processing section contains modulation and demodulation process in digital manners.

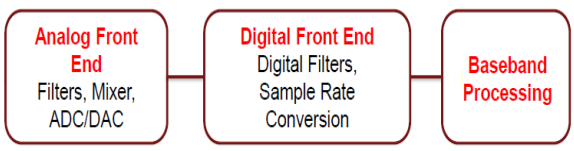

Fig. 1. Functional Block Diagram of SDR Technology

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There are many researcher has been propose efficient investigation of SDR transceiver model based on QAM techniques with optimum performance. The carrier synchronization of SDR transceiver based signal processing has introduced by [7]. The carrier recovery of QAM and QPSK modulation over FPGA is developed. This suggestion examines the maximum likelihood in the phase of carrier in QAM scheme which is implemented in FPGA vertex-4. Because of QAM signal is dependent data, the detection of the amplitude and phase should insert the modulation in the receiver part and generate proportion of signal depend on phase different among local quadrature carrier and received data. His implementation of high performance digital system has made advance process technology. The approach of SDR model design has been prepared by [8] for software wireless communication system. His work optimizes the synchronization for hardware efficiency in both carrier and phase offset with timing recovery technique optimization. A novel low power consumption QAM scheme using logic gates has been projected by [9]. Low power data path design and QAM utilize framework compared with existing mode is developed and examined as well in that woks. In this research, the short cycle design of SDR transceiver has been suggested were examined and investigated sufficiently. The design flow support the designer to implement his work under SIMULIK block set environments with HDL optimization easily. The suggested approach could decrease the time required to implement in hardware and give better understanding about different design. Figure 2 show the proposed flow chart to implement the optimized HDL code for SDR transceiver based QAM scheme in FPGA module.

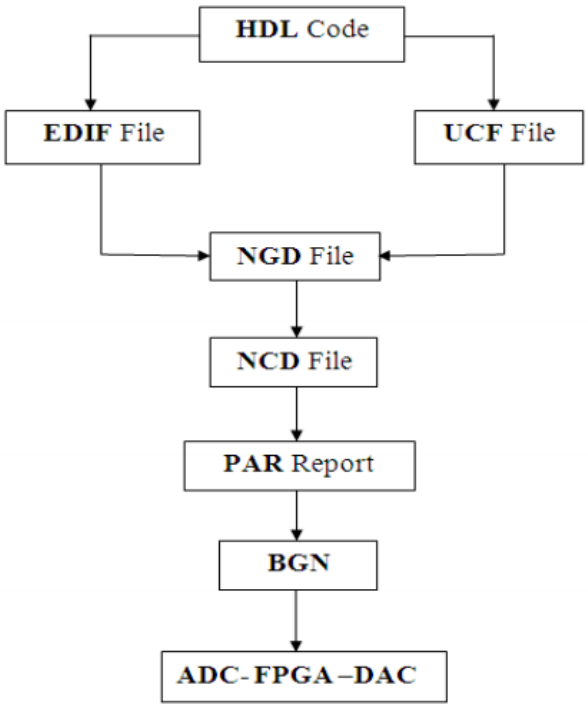

Fig. 2. Flow Chart of HDL Code Implementation

2. SDR Transceiver Design in MATLAB

The optimized HDL of QAM transmit and receive data system shown in Figure 3 has been prepared and simulated in MATALB as first step in implementation process. This model could be used later for HDL code generation in baseband section for digital wireless systems. In transmitter part, a complex value of HDL 64-QAM data was generated in floating point mode to send via AWGN channel. This channel is used to add noise, attenuation, carrier frequency offset and fractional delay in order to demonstrate and examine the receiver performance with these conditions. The receiver system simulates the practical receiver and moderate the channel effects depend of time and frequency recovery techniques. The frame synchronization under phase and magnitude recovery was done properly. The decoded techniques of the received information packet were printed to command window of MATLAB programs by text decoding system.

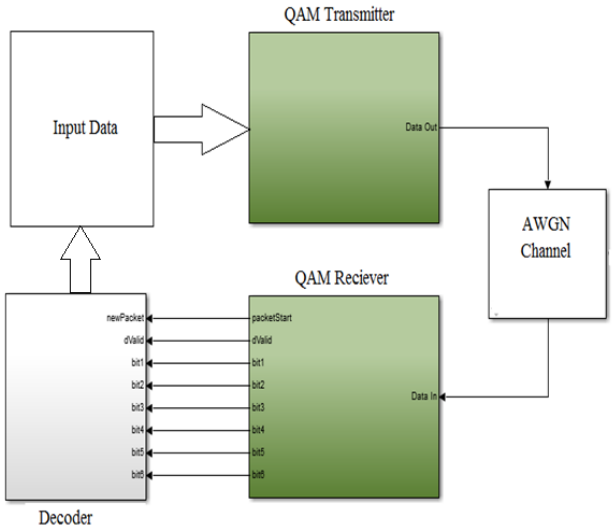

Fig. 3. SDR Transceiver Model Based QAM Scheme

The structure of top level QAM transmitter shown in Figure 4 has been optimized for code generation in subsystem to use for HDL written in command window. This section consists of data generation block, the symbol mapping block and pulse shaping filter. The generated of data packets is transmitted in form of grouping bits for symbol mapping. The map of output bits in form of QAM is generated which sent to shaping filter. Then, the pulse shaping will perform and up-sampled the symbol by using RRC filters as an interpolator before transmitting.

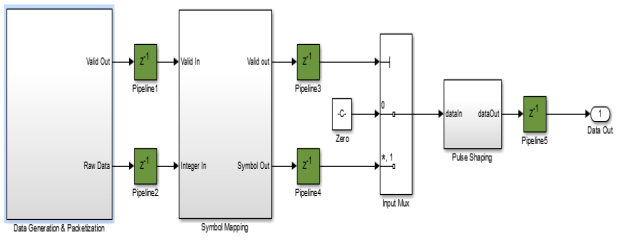

Fig. 4. Transmitter Subsystem of SDR Model

The channel used in this model is anticipated to be a routing approximation of AWGN with frequency offset and attenuation which is running under software form and not support to generate the HDL code. Additionally, this block dose not supports the fixed point data and the conversion to double precision data should take into account in this case. The gain block is used to attenuate the transmitted signal and

fractional delay has been applied. The high level block of QAM receiver design could be illustrated in Figure 5.

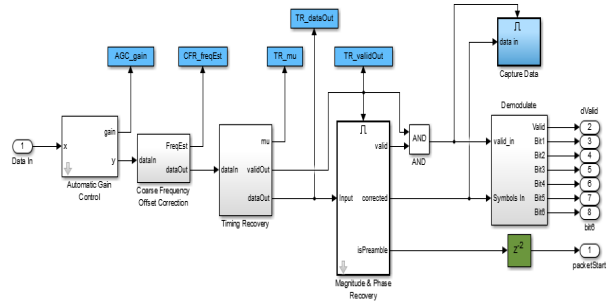

Fig. 5. Receiver Subsystem SDR Model

The optimize model of QAM receiver consist of automatic gain control and magnitude / Phase Recovery modules as well as demodulation block. The AGC circuit used to normalize the power of received signal in term of frequency offset correction by estimation of approximate value and then correction is formulated. The RRC receiver filter is used to down sampling the income signal from channel. To resample the received signal, the timing recovery block is used to recover the time strobe to decide whatever the correct symbol is optimize the sampling instant or not. To perform the packet detection and fine gain, the magnitude and phase recovery is used in the receiver part. The fine gain of phase and magnitude correction is performed by this recovery subsystem also. The demodulator block is used to demodulate the income signal and de-mapping the symbol to bits form. The decoding of text message could be established by using the text message decoding block shown in Figure 6.

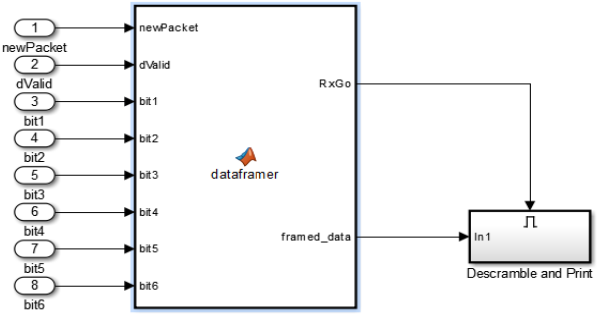

Fig. 6. Decoding Block Subsystem in Receiver Part

The text decoder expected to run in software to employ frame based signal accelerate and optimize the computation process. The output of QAM receiver is 8 sample signals and the valid signal is represented from bit 1 to bit 6 as Boolean signal. The data framer in the receiver is used to convert the signal from sample based to frame based. The valid port is set to high state to demodulate the bits and data frame block is used to fill up the delay line according to bits. New data packet signal is forward this data and stored in the delay line in order to reset the delay line. The received data is descrambling when the block is enable when either delay accumulate 336 valid demodulated bits.

3. HDL Optimization

The task of HDL optimization of QAM transceiver under SDR technology shown in Figure 7 could be summarizing as below:

a. The finite state machine is used to control and optimize the data generation by scramble the data bits and built the packets which contain of 84 barker code bits and 252 data scramble data. The block of group bit convert the input data to six integer bit with 1/6 of input sample rate which is required by sample mapped.
b. The pipeline delay of 2 samples is used in data source block which insert between data source and bit pairing. Therefore, the data will be delayed to be close the pipeline delay in the path of information. To reduce the sample rate, the group bit is used in this section and down sampling by 6.

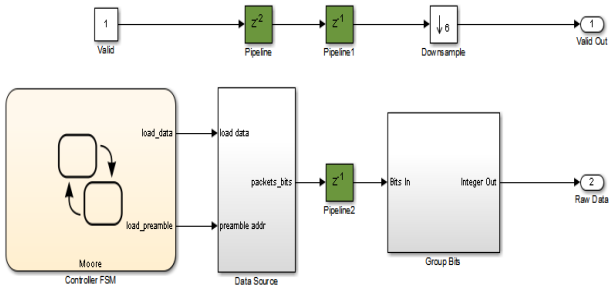

Fig. 7. HDL Optimization structure of HDL QAM transceiver

The finite state machine was control the system by so called Moore state machine using the capability of state flow chart from math works which contain three states, pack preamble 1, 2 and append data flow to serve the adder output from 0 to 83. After that, the FSM change the status to append data and the Boolean forms which are used to enable the counter controller of data into packet frame. Two look up table and data bits is the main component of data source system which is directly addressed by controller the FSM through address signal. Each data LUT is addressed by counter and HDL counter to enable by data load signal which is produced by FSM controller to ensure the proper clock cycle numbers. The preamble of LUT is directly addressed as serial in every packet for LUT data to be varied in every packet as different bits. The optimized data source scheme sown in Figure 8 is used in this model.

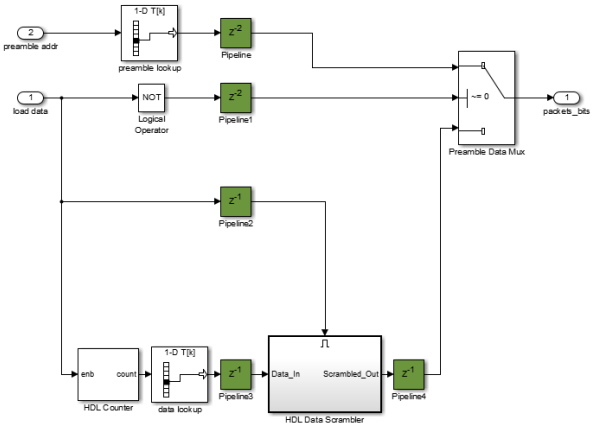

Fig. 8. optimized data source model

Figure 9 shows the HDL data scrambler which is design from register and XOR gates to enable and ensured the scrambler is only enabled at what time there is original input data is processed. The scrambler shall generate bit streams in continuous mode to output bits at the same rate of transmit bit rate. There is constantly scrambler in digital transmission systems to scramble the data after multiplexing process before transmission which is descrambled and de-multiplexed in the receiver side in serial mode. The scramblers used to transform the input data stream by applying the binary sequence and stored in the read only memory. In this case, the sync word is used to ensure the synchronous operation of transmit and received data which is scramble and descramble earlier. The encrypting data and adequate message security is scramble and descramble to decrease the cost and improve the data security with large number of shift register. However, any increasing of sequence generator stages resulting in significant increasing in the security of message. While, any increasing in hardware to enhance the security of scrambler is achieved by using conventional integrated circuit. Hence, in proposed scheme, the scrambler and descrambler is implementing by use HDL to optimize the design and lead to perfect synchronization between receiver and transmitter.

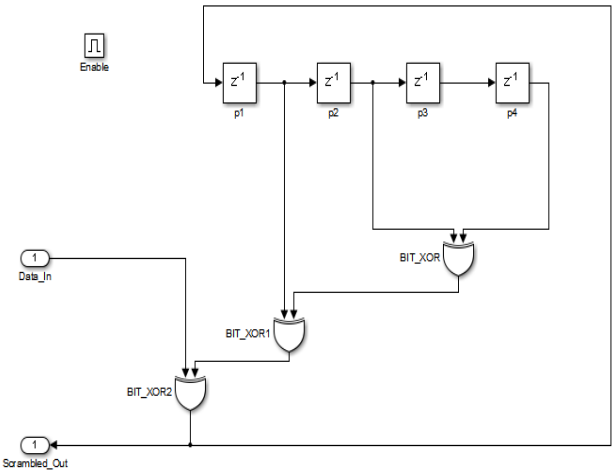

Fig.9. optimized HDL data scrambler

The group bite is used to produce six bits from six individual bit as unsigned integer output which expected to be symbol mapping components in the stat flow path. To align six bits to the input, the delay unit is used to concatenate it into six bit unsigned output bits which is down sampled in next stage in order to choice a correct group of bits. To optimize the HDL QAM receiver, the AGC, timing recovery and frequency offset should be projected to be optimized as illustrated in Figure 10. The AGC logarithmic loop is used to decrease the error. Hence, the output signal is a product of the input signal and the exponential of loop gain in the circuit. The different between reference level and product of logarithm of detector output and the exponential of gain loop. Then, after the multiplication by step size, the AGC passes the error signal to the integrator to generate correction signals. Therefore, to provide high level performance for variety of signal type including modulation process, the AGC loop has been used. Compared with conventional AGC, the detector is applied to the input signal to increase the convergence time and signal power variation at the input of detector because the large variation in floating point design is neglected.

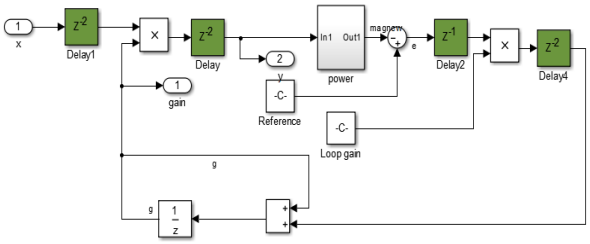

Fig 10. AGC optimization model

To estimate and correct the frequency offset, the Luis algorithms have been used in the receiver optimization techniques which make estimation depend on the output of RRC filter as shown in Figure 11. Then, the RRC filter input will correct to ensure that the interested part of received signal bandwidth is valid. Additionally, the SNR will be compensated compared with correcting output of RRC filter. The correction technique was operated in close loop to make an updating of last estimated frequency and in the same manner the estimating process will done properly. The implementation of estimating average was containing in the loop gain as describe in [10]. The down sampling technique is implemented by RRC filter which is important for up sampling as feedback signals by use repeated block as well as rate matching for filter input. Due to clock variation between transmitter and receiver, the frequency synchronization module enables the receiver to overcome the frequency offset problems. In the proposed technique, the frequency offset algorithm has been implementing between the input and output to estimate the frequency by mean of channel estimation block. The fine frequency offset and fine symbol timing offset estimation is relying on the legacy long training field (L-LTF) which is composed of the cyclic prefix and two identical long training symbol

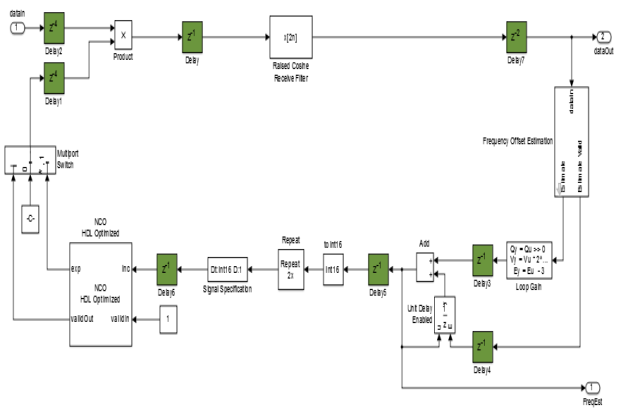

Fig. 11. Frequency Offset Estimation

The optimization of timing recovery technique shown in Figure 12 has been used in the receiver part as a major process in the receiver. In order to generate the control signal, the facilitate interpolation is chosen to selected the filter type and this control signal is used to enable time detectors. The timing error calculation will correct the time instant in this case and the interpolation control was updated the time difference. The filter used in interpolation process design is planned as all filter coefficients become 1,-1/2, 3/2

to facilitate and optimize the structure of filter. Time error is produced using zero crossing detectors as describe in [11].

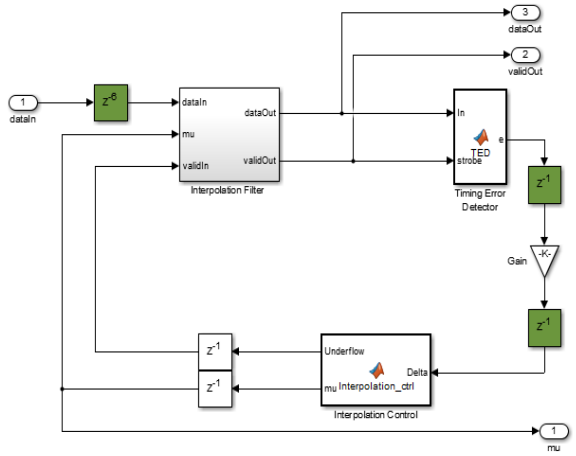

Fig. 12. timing recovery scheme

4. Results Discussion and Analysis

When the model were running, the display of received data is productively shown the results of optimum simulation for QAM transceiver performance. Figure 13 illustrate the activation of gain control in AGC circuit to the normalized output behavior. When the gain was reach to relative level, the plot will shows the number of ripple as well as the speed of AGC request to control the simulation and keep stable the balance between input and output signals. So, when large loop gain is adapted, the speed varies high and when the loop gain adapted small gain, the level of smoothing take more time to adapt.

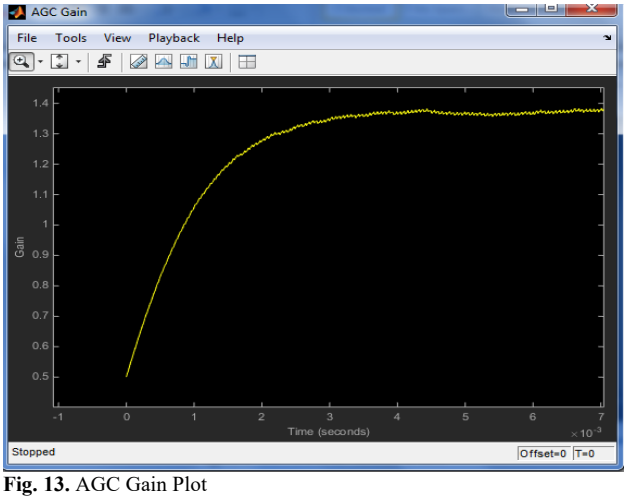

Fig. 13. AGC Gain Plot

To show how the coarse frequency offset is steadily adapt toward frequency offset of the system, Figure 14 illustrate the estimation come close to the actual frequency. In this plot one can see that the residual error is still appear which should addressed in the system and eliminate this error properly.

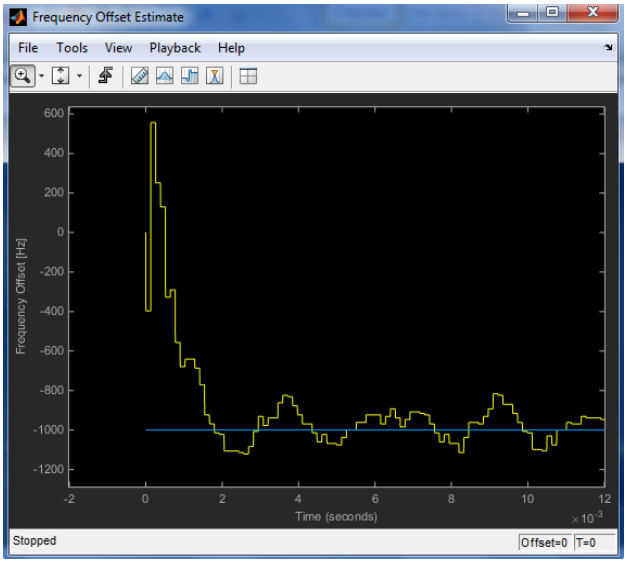

Fig. 14. Estimated of frequency offset plot

Figure 15 showing the interpolation filter timing recovery which reaches to stable case with the time when the delay of the channel is not change during the model running.

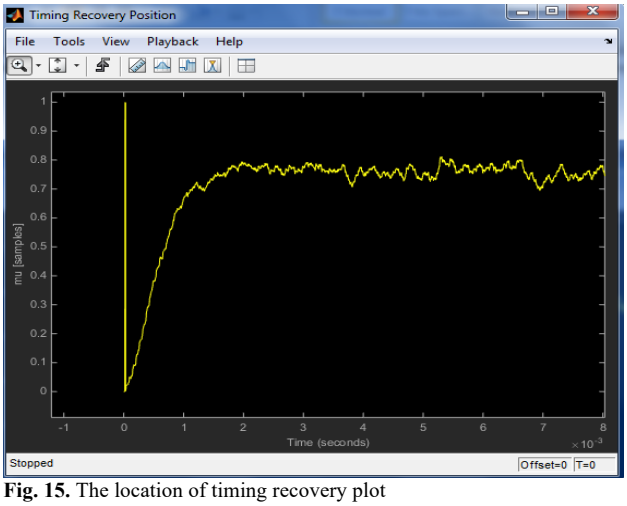

Fig. 15. The location of timing recovery plot

Figure 16 show the real time part of QAM timing recovery starting to cover the eight amplitude values expected in 64QAM scheme. Thought, when the residual frequency remain not corrected, the quality of signals was varies with amplitude level and clearly appear in some points and the constellation remain has some rotation.

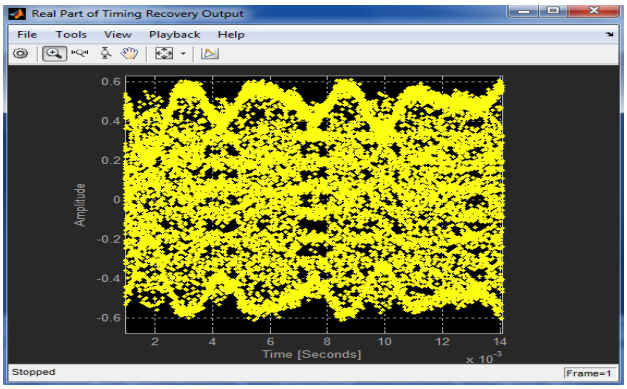

Fig. 16. Timing recovery output of real time part of QAM schem

Figure 17 illustrate the magnitude and phase adaptation with time which appears after fine frequency recovery and then the constellation must not rotate in this point. One could see the eight amplitude levels represented by eight real amplitude levels in 64 QAM scheme. The size of each constellation points should be reduced by decrease the channel noise because any increasing of channel noise will merge together a lot of constellation points in this case. The rotation of constellation is appear clearly in this plot due to successful corrected the frequency offset in this design.

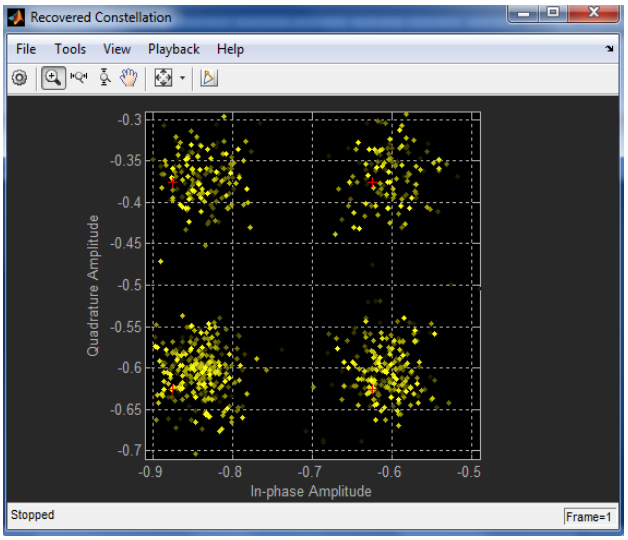

Fig. 17. The constellation of time recovery plot

5. Conclusion

This paper introduces successful design of HDL Optimization in SDR Transceiver Based QAM Scheme to be use in wireless systems. The obtained simulation results proof that the transmitter data has been matched with receiver output with minimum errors with low cost and power consumption due to use SDR technology usage in the suggested structure. Better performance and flexible customizing for different information rate have been provided with different modulation and filter type which achieve effective and reconfigure design. Many specification and different requirements of design could be provided under SDR technology with chip reprogramming and reconfigure. This technology could easily optimize the HDL design for FPGA implementation utilization to support the wireless system. The proposed error coding and decoding need further investigation and improvement to decrease and optimize the error between transmitted and received data. This paper introduces promising HDL optimization to accelerate and support the new generation of communication system like cellular and global positioning.

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