

Research Article

Model of DC/DC Dual-Bridge Series Resonant Converter in Buck and Boost Modes for Output Current and Commutation Timing ControlAlex Borisevich^{1,*} and Filipp Gleyzer²¹BrutBio Inc.²Department of Automotive, Skyline College, 3300 College Drive, San Bruno, CA 94066, USA.

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Abstract

In the paper, a control-affine model for the active dual-bridge series resonant converter is presented. The model has square form and produces cycle averaged output current and two parameters of waveform alignment for the controllable achievement of ZVS and synchronous rectification. The output characteristics of the converter are obtained by using the first harmonic approximation of input voltage applied to the resonant tank. The maximum prediction error of this model is about 10% in comparison to the measured data. This model is suitable for both voltage buck and boost operations, and also demonstrates fundamental control properties of the converter namely high nonlinearity respect to the control inputs, a singularity of output current surface between buck and boost modes, and holonomic constraints for control variables.

Keywords: Protein adsorption; bovine serum albumin; nickel-titanium; pyrogallol; tannic acid

1. Introduction

The dual-bridge series resonant converter (DB SRC) [1], which shares some similarities with the standard full-bridge DC/DC series resonant converters (like LLC), still has some unique features due to the secondary-side bridge, such as the capability of bidirectional power flow and voltage boost operation. Such type of converter topology is particularly promising for electric vehicles chargers applications [1-3], including off-board charging stations and on-board charger modules with an ability for bidirectional vehicle-to-grid power flow. Additionally, many other power electronics applications like battery energy storage and DC line power transmission are target areas of DB SRC topology.

The modulation scheme for DB SRC usually enables pure ZVS on the primary side, and combined ZVS/ZCS on the secondary side, and allows for an efficient utilization of the primary side switches with wide changes in load or supply voltage, which is preferred in many applications [2]. The impedance of series resonant tank is determined by value of inductor and capacitor together with the switching frequency. Therefore, it can operate at higher frequency under high power level [3] than just dual active bridge topologies without resonant capacitor, which allows more compact magnetic designs.

All the switches in the two bridges work with 50% duty cycle, but have a phase shift between the two bridges [4]. The switching frequency is set higher than the LC resonance frequency, thus, the converter works only in continuous current mode. The amount of power transfer is controlled using the phase-shift angle, whereas, the power flow direction is dependent on the polarity of phase shift.

Comparing to LLC converter, the DB SRC converter

requires more advanced control strategy since the DC gain of a LC series resonant converter is always less than unity with a passive (diode) rectifier. Also at light-load condition, the impedance of the load is very large compared to the impedance of the resonant network, so all the input voltage is imposed on the load [5]. Thus an actively controlled full bridge on the secondary side is essential in order to achieve voltage gain higher than one and regulate power delivered at light load.

The operating modes and controls principles of the converter have been extensively analyzed in [6, 7, 8]. The published modeling efforts can be classified into three categories:

1. Fundamental harmonics approximation (FHA) approach [6, 7, 8, 9, 10], consisting of replacement the rectangular voltage waveforms by sinusoidal approximations, calculated accordingly. The same result can be achieved if output and input voltages are represented by rotating vectors using phasor diagrams. If the analysis of a converter is performed not too far from its resonant frequency, then the resonant tank current consists primary a fundamental harmonic, and this method produces reasonable well approximations. Another advantage of FHA is that this method ends up with trigonometric functions over switching parameters, where analytical results can be relevantly easy to obtain.
2. State-plane trajectory analysis pioneered by R. Oruganti [12] and used by many followers [13, 14, 15, 16]. The key idea is to represent the converter dynamics in two-dimensional plane of resonant inductor current and resonant capacitor voltage. The analysis is greatly simplified by the fact that with a proper normalization the state plane trajectory of voltage step response of an undamped LC circuit is circular and is centered at the DC solution of the

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circuit. Thus, accurate and purely geometric analysis can be performed for arbitrary operating point and switching pattern. The downside of this method is that the closed form solutions are becoming very complicated with less trivial PWM patterns (like combined duty cycle and phase shift control), and also for multi-element resonant converters, more state variables need to be analyzed and more complicated calculation is required.

3. Piece-wise time-domain modeling. This technique is originally applied to the dual-bridge converters [17, 18, 19, 20] without a resonant tank, where transformer current is a straight line between switching events. Thus each time interval between switching of bridges can be analyzed separately, and then final waveform is obtained by gluing together transient responses for consequential time intervals. This technique can be directly obtained to series resonant converter operating very far from resonant frequency, where resonant tank current is piece-wise linear. Also it is not very hard to obtain a closed form solutions for different operating modes of series resonant converter [21].

Despite pretty diverse modeling and control techniques published, there are still some gaps, namely:

- there is no model and corresponding nonlinear control problem formulated addressing both produced output power and optimal regime of operation in terms of the waveform timings,
 - all three modes of operation, namely variable frequency buck, variable frequency boost and fixed frequency low power operation are not being considered in a single model.
- In this work we will derive nonlinear control affine model of the converter, which describes large signal operation over whole frequency range above resonance and in all possible operation modes as buck, boost and low power. This model also demonstrates interesting control properties of the converter like high nonlinearity respect to the switching parameters, singularity of output current surface between buck and boost modes, and also holonomic constraints for control variables. We believe that this model could be an another practical benchmark for many advanced nonlinear control techniques such as feedback linearization, differential flatness theory, optimal control, etc.

2. Circuit representations

The basic electrical circuit of the series LC resonant DC/DC converter is shown in Figure 1.

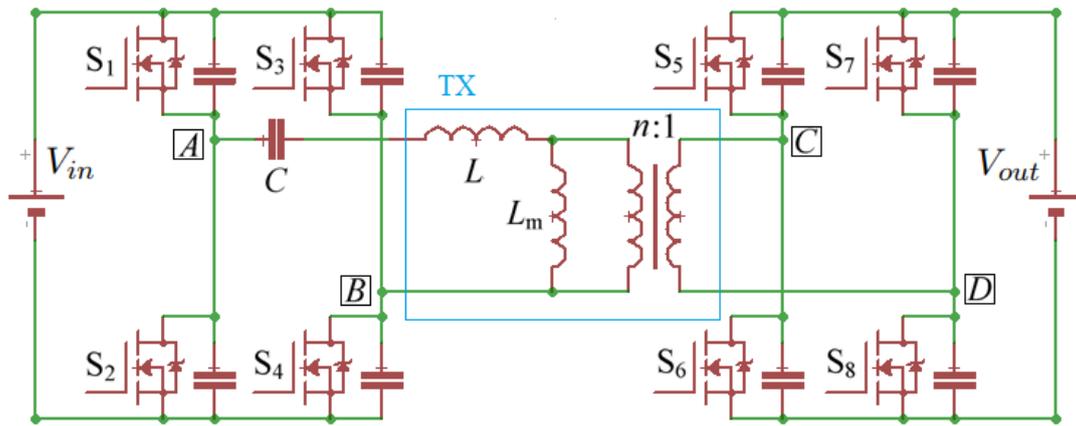


Fig. 1. Topology of series LC resonant DC/DC converter.

The circuit consists of two full (H) transistor bridges: input bridge with switches $S_1 - S_4$ and output bridge with switches $S_5 - S_8$. The output bridge is directly connected to the secondary side of transformer TX. The input bridge is connected to the transformer TX through capacitor C. Simple representation of transformer is used with magnetizing inductance L_m , leakage inductance L and an ideal transformer with turns ratio n .

If the magnetizing inductance L_m is much larger than leakage inductance L : $L_m \gg L$, then there is almost no circulating magnetizing current in the circuit. This has an advantage because all the current from primary side is flowing to the secondary side which increases the efficiency. Also the current in secondary side of transformer is in phase with primary side, which allows easy synchronous rectification by measuring current only in primary side.

By eliminating L_m from the circuit, we can spot that the stray inductance L together with capacitor C forms LC resonant tank. Also ideal transformer can be embedded into secondary bridge for simplification of analysis. Thus we

can obtain a black-box circuit presented in Figure 2. Should be noted that we will not introduce lumped circuit component for losses modeling, however control design should be carried out with keeping in mind minimization of current $i_t(t)$ between bridges, which corresponds to minimization of conduction losses for switches. Also in subsequent discussion we will show how to achieve ZVS turn-on switching for all devices. But the turn-off losses can be only mitigated by connecting capacitive snubbers across all switches in addition to their intrinsic C_{oss} capacitance.

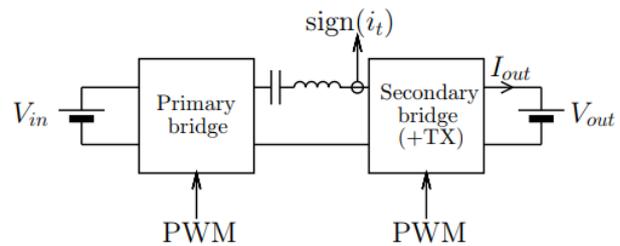


Fig. 2. Representation of DC/DC converter using abstracted bridges.

The bridges can be represented as pulsed voltage

sources, with voltage shapes controlled by a PWM pattern. The amplitude of voltage $v_{in}(t)$ for input bridge source is equal to V_{in} , and the amplitude of voltage $v_{out}(t)$ for output bridge source is equal to $n \cdot V_{in}$, where n is transformer turns ratio. Figure 3 shows the representation of DC/DC converter using voltage sources as bridges.

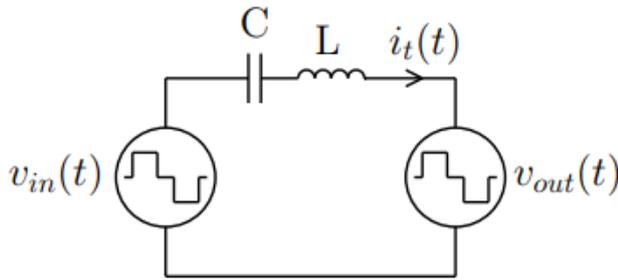


Fig. 3. Representation of DC/DC converter using voltage sources as bridges.

3. Switching Waveforms

Let's consider voltages $v_{in}(t)$ and $v_{out}(t)$ at output terminals of bridges. In the circuit at Figure 1 this corresponds to voltage measured between points A-B for input bridge and scaled n times voltages between points C-D for output bridge. Effectively, these are the voltages applied to LC-circuit. Figure 4 shows the real (top) and rectangular approximated (bottom) voltages.

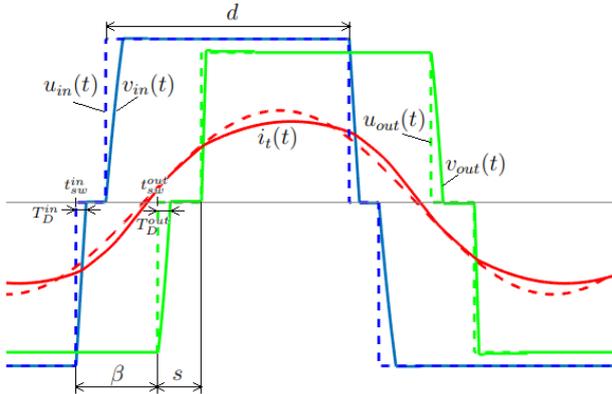


Fig.4. Real and approximated voltages applied to resonant LC circuit and commutation parameters.

Let's consider rectangular approximated voltages $u_{in}(t)$ and $u_{out}(t)$ for easier explanation of controllable switching parameters:

- The input voltage source is producing rectangular pulses with controlled duty cycle and frequency. The amplitude of pulse is V_{in} and the on-time is d (in radians, i.e. $d = \pi$ is full square wave). The angular frequency is ω , which is equivalent to frequency $F = 1/T$ in Hz.

- The output voltage source is producing rectangular pulses with amplitude nV_{out} with controlled duty cycle, frequency, and phase shift respect to input bridge. The reciprocal of duty cycle, the off-time or short time is s (defined in radians, $s = \pi$ means that secondary side of transformer is fully shorted). The off-time is always located at the beginning of switching cycle. The phase shift between

the output bridge switching cycle and input bridge switching cycle is β .

The output to input voltage ratio is defined as converter voltage gain:

$$G = \frac{nV_{out}}{V_{in}} \quad (1)$$

The real waveforms are looking differently than approximated ones because of dead times, which are smoothing rising and falling edges of the switching pulses. Since this DC/DC belongs to the class of resonant converters, energy is also transferring during the dead time, and the dead time is an essential phase of converter operation.

The duration of dead-time for input bridge is T_D^{in} , and the duration of dead-time for output bridge is T_D^{out} .

4. Turn-on ZVS conditions

The zero-voltage switching (ZVS) condition for turn-on means that at a moment of physical closing (turn-on) of the switch, the voltage across it should be negligible. For the many converters including considerable one this means that the body reverse diode of the switch starts to conduct at the end of dead-time, and the commutating voltage is just a body diode voltage drop. The implementation of this principle implies that the alignment of a waveform and a switching PWM pattern allows the current which is freewheeling during dead-time current to discharge capacitor across the device which is going to turn-on after this dead-time.

By a little bit more detailed circuit analysis (which is out of the scope of this paper), following condition for the ZVS switching in the primary input bridge can be imposed:

$$-\frac{1}{2C_{ds}^{in}} \int_{t_{sw}^{in}}^{t_{sw}^{in} + T_D^{in}} i_t(t) dt > V_{in} \quad (2)$$

where C_{ds}^{in} is equivalent capacitance across the transistor to be switched, and t_{sw}^{in} is a moment of the start of dead-time.

Practical conclusions from (2) are: the current $i_t(t)$ during dead-time should be negative enough, and the duration of dead-time T_D^{in} should be long enough.

Similar condition for the output bridge:

$$\frac{n}{2C_{ds}^{out}} \int_{t_{sw}^{out}}^{t_{sw}^{out} + T_D^{out}} i_t(t) dt > V_{out} \quad (3)$$

where C_{ds}^{out} is equivalent capacitance across the transistor to be switched, and t_{sw}^{out} is a moment of the start of dead-time.

Practical conclusions from (3) are: the current $i_t(t)$ during dead-time should be positive, and the duration of dead-time T_D^{out} should be long enough.

5. Primary and Secondary Waveforms Alignment

Conditions in form of (2) and (3) are not practical enough for controls implementation. Let's find out necessary conditions to satisfy (2) and (3) by considering an alignment of input and output voltages respect to the moment of zero current $i_t(t) = 0$ presented at Figure 5.

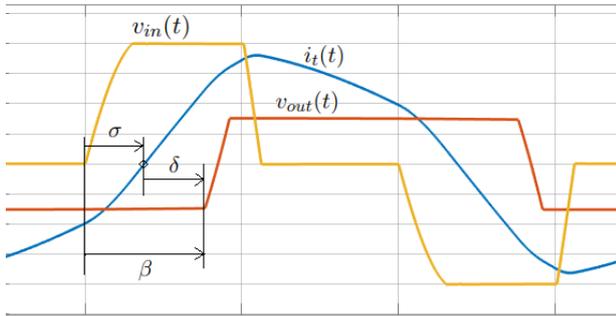


Fig. 5. Alignment of input and output voltages respect to zero current crossing.

Let's denote σ as an angular duration between rising edge of input voltage $v_{in}(t)$ and the moment when rising current $i_t(t)$ becomes zero. Also let's introduce δ as an angular duration between the moment when rising current $i_t(t)$ became zero and beginning of output bridge switching cycle (for the particular waveform at Figure 5 this corresponds to the rising edge of output voltage $v_{out}(t)$ because $s = 0$ here, i.e. secondary bridge is fully driven). It is obvious that:

$$\sigma + \delta = \beta \tag{4}$$

Thus we can formulate following necessary ZVS conditions for primary and secondary sides:

$$\begin{aligned} \sigma &\geq \sigma_{min} \\ \delta &\geq 0 \end{aligned} \tag{5}$$

It is possible to show that the necessary conditions can be satisfied by additionally ensuring that the dead-time durations T_D^{in} and T_D^{out} are also long enough.

The alignment of resonant current $i_t(t)$ and output voltage $v_{out}(t)$ is also very important for an active power delivery to the load, which essentially impacts converter efficiency. The average output power delivered during a half of switching period T can be calculated as

$$P_{out} = \frac{2}{T} \int_0^{T/2} v_{out}(t) \cdot i_t(t) dt \tag{6}$$

By assuming that the current is zero at initial time moment, i.e. $i_t(0) = i_t(T/2) = 0$, and also approximating the output bridge voltage by rectangular waveform of amplitude nV_{out} , the power can be separated to negative and positive parts during half of switching period:

$$\begin{aligned} P_{out} &= \frac{2}{T} \left(\int_0^{T_\delta} v_{out}(t) \cdot i_t(t) dt + \int_{T_\delta}^{T/2} v_{out}(t) \cdot i_t(t) dt \right) \\ &= \frac{2nV_{out}}{T} \left(-\int_0^{T_\delta} i_t(t) dt + \int_{T_\delta}^{T/2} i_t(t) dt \right) \end{aligned} \tag{7}$$

where $T_\delta = \delta / \omega$ is a moment when output bridge voltage changes its sign from negative to positive.

It is obvious that in order to maximize the delivery of output power and as a result maximize the converter efficiency (since less amplitude of tank current is needed to deliver the same amount of power, i.e. less conduction losses) the negative part of P_{out} should be zero, or $T_\delta = 0$ or

$$\delta = 0 \tag{8}$$

Finally the combined ZVS and maximum power delivery conditions can be formulated together:

$$\begin{aligned} \sigma &\geq \sigma_{min} \\ \delta &= 0 \end{aligned} \tag{9}$$

with addition of dead-time constraints:

$$\begin{aligned} T_D^{in} &\geq (T_D^{in})_{min}, T_D^{out} \geq (T_D^{out})_{min} \\ i_t(t_{sw}^{in} + T_D^{in}) &\leq 0 \end{aligned} \tag{10}$$

The last inequality ensures that the sign of tank current will stay negative during whole dead-time for primary side bridge to prevent capacitor across the device to be charged again by positive direction of current. It implicitly constrains both σ_{min} and $(T_D^{in})_{min}$.

6. Approximation of steady-state regulation characteristics

To get a better understanding of regulation characteristics as a dependency of output current I_{out} from voltages and switching parameters, let's perform first harmonic approximation of voltage applied to the LC resonant tank. Considering voltages $u_{in}(t)$ and $u_{out}(t)$ pictured at Figure 4 and resulting voltage $u(t)$ at Figure 6, the first harmonic approximation of $u(t)$ can be calculated as:

$$\begin{aligned} u(t) &= u_{in}(t) - u_{out}(t) \approx \bar{u}(t) \\ \bar{u}(t) &= \frac{V_{in}}{2\pi} (A \cos(\omega t) + B \sin(\omega t)) = \frac{V_{in}}{2\pi} \sqrt{A^2 + B^2} \sin(\omega t + \varphi_0) \\ A &= 4 \sin d + 4G \sin(\beta + s) + 4G \sin \beta \\ B &= 4 - 4G \cos(\beta + s) - 4G \cos \beta - 4 \cos d \\ \varphi_0 &= \arctan(A, B) \end{aligned} \tag{11}$$

where arctan is two-argument arctangent function, and coefficients A and B are obtained by taking first Fourier series coefficients of $u_{in}(t)$ and $u_{out}(t)$ with subsequent collection of terms.

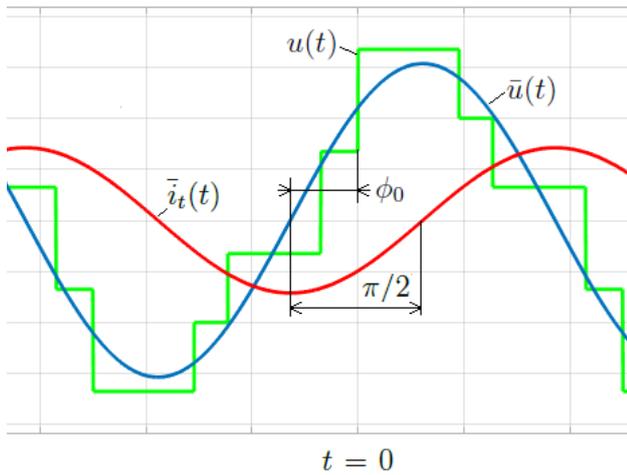


Fig. 6. First harmonic approximation of applied to the resonant tank voltage and resulting current.

Very important to keep in mind that initial moment of time $t=0$ in (11) coincides with the rising edge of input voltage $u_{in}(t)$ as it shown in Figure 6..

The first harmonic approximation of current $\bar{i}_t(t)$ is given by AC circuit theory fact:

$$\bar{i}_t(\omega t) = \frac{1}{Z(\omega)} \cdot \bar{u}(\omega t - \pi/2) \quad (12)$$

where

$$Z(\omega) = X_L - X_C = \omega L - \frac{1}{\omega C} \quad (13)$$

The amplitude of tank current is determined from (12) and (11) by:

$$I_i = \frac{V_{in}}{2\pi Z} \sqrt{A^2 + B^2} \quad (14)$$

Let's determine alignment parameters of waveforms σ and δ . It is obvious from the picture that:

$$\sigma = \frac{\pi}{2} - \varphi_0 \quad (15)$$

And since $\sigma + \delta = \beta$, the δ parameter is

$$\delta = \beta - \sigma = \beta - \frac{\pi}{2} + \varphi_0 \quad (16)$$

The remaining question is how much current is flowing to the load through the output bridge. The current appeared at the secondary side of transformer is $n \cdot \bar{i}_t(t)$. To calculate the average (DC) value of the current we should account a negative portion of the power during interval δ , as well as no current flow during shorting interval s and actual positive power delivery during $\pi - \delta - s$, as it pictured in Figure 7.

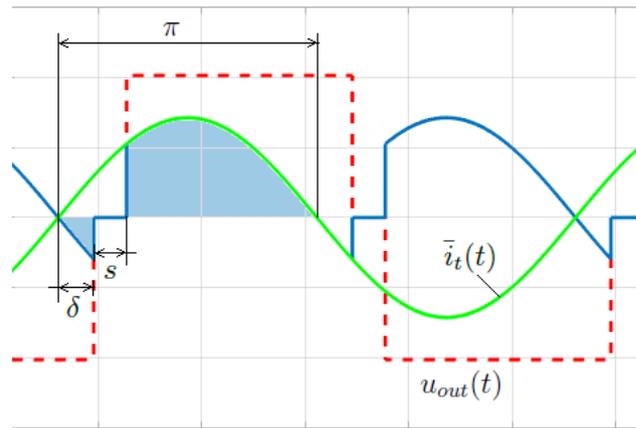


Fig. 7. Principle of I_{out} calculation.

Without the loss of generality, lets align integration interval with a moment of zero crossing $\bar{i}_t(0)=0$. The average value of current is:

$$I_{out} = \frac{nI_t}{\pi} \int_0^\pi \sin \varphi \cdot (u_{out}(\varphi)) d\varphi \quad (17)$$

or

$$I_{out} = \frac{nI_t}{\pi} \left(-\int_0^\delta \sin \varphi d\varphi + \int_{\delta+s}^\pi \sin \varphi d\varphi \right) \quad (18)$$

and finally

$$I_{out} = \frac{nI_t}{\pi} (\cos(s+\delta) + \cos \delta) \quad (19)$$

It is convenient to normalize the output current of converter to input voltage by considering input to output transconductance:

$$W = \frac{I_{out}}{V_{in}} = \frac{n}{2\pi^2} \frac{\sqrt{A^2 + B^2}}{Z} (\cos(s+\delta) + \cos \delta) \quad (20)$$

In that case, it is possible to analyze converter characteristics only in terms of relative quantities which are independent from specific input and output voltages, i.e. only using voltage ratio G and transconductance W .

8. Input-output representation and affine nonlinear model

In this section we will assume that primary side is always fully driven:

$$d := \pi \quad (21)$$

This brings the PWM modulation scheme closer to the control of LLC converters. However for a low-power mode when the frequency is clamped to the maximum value, it might be not an optimal strategy, which could be addressed separately.

With $d = \pi$, the coefficients from (11) can be simplified further:

$$\begin{aligned}
 A &= 4G \sin(\beta + s) + 4G \sin \beta \\
 B &= 8 - 4G \cos(\beta + s) - 4G \cos \beta \\
 \tan \varphi_0 &= \frac{A}{B} = \frac{\sin(\beta + s) + \sin \beta}{2 / G - \cos(\beta + s) - \cos \beta}
 \end{aligned}
 \tag{22}$$

Thus we have three inputs of the plant: ω , β , s and three outputs: W , δ , σ which makes the system input-output square and potentially invertible (Figure 8). The voltage ratio G is an external non-controllable parameter.

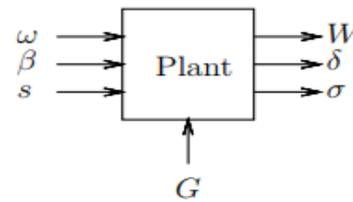


Fig. 8. Input-output representation of the resonant converter model.

The outputs W , δ , σ of the system are governed by the equations (20), (16), (15) respectively. The nonlinear maps (20), (16), (15) can be visualized in more details using Simulink blocks as pictured at Figure 9.

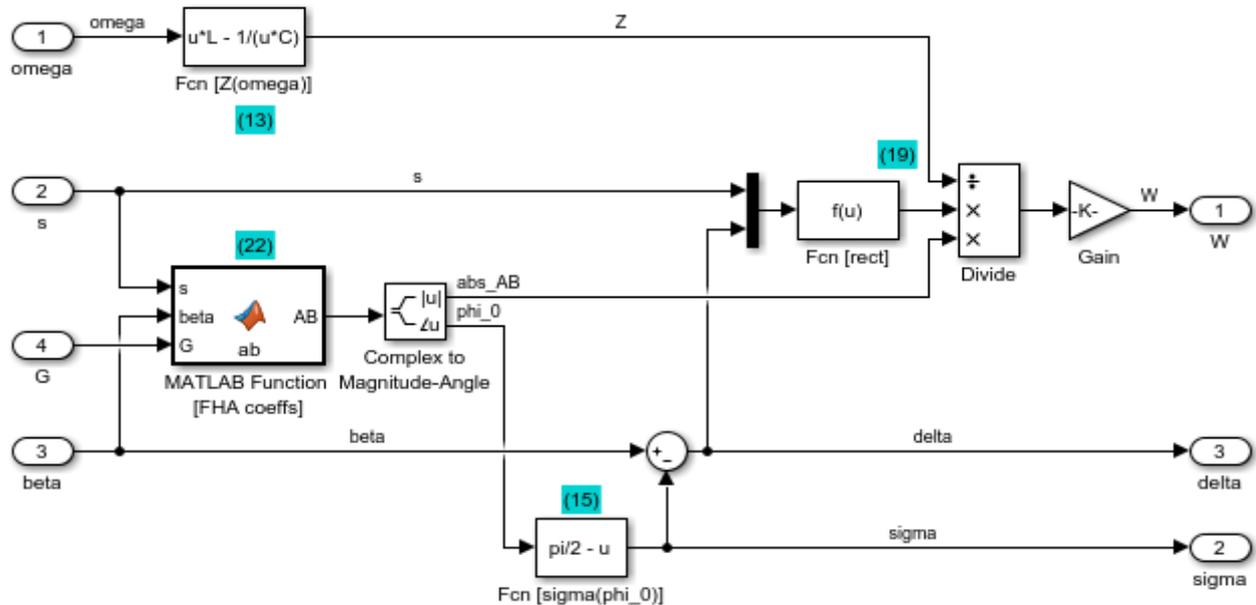


Fig. 9. Detailed representation of the converter model using Simulink block (text in blue color is equation number).

In order to formally produce control affine nonlinear model of the converter in form of

$$\dot{X} = f(X) + \sum_{i=1}^m g_i(X) \cdot U_i, Y = h(X)
 \tag{23}$$

the control inputs ω , s , β can be passed through integrators, making the system differentially controllable by corrective actions rather than using absolute values. Thus, the function h is vector-valued given by (20), (16), (15), and dynamical part of the plant given by $f=0, g_i=1$ are describing individual integrators only. Worth noting that another option to introduce dynamics to the model is consider simple first order delays for control inputs ω , s , β , which could model slew rate limiters as filters or simply a command propagation delay through the software chain and PWM modulator.

Finally, we can write down the complete model:

$$\begin{aligned}
 W &= \frac{n}{2\pi^2} \frac{\sqrt{A(\beta, s, G)^2 + B(\beta, s, G)^2}}{Z(\omega)} (\cos(s + \delta) + \cos \delta) \\
 \delta &= \beta - \frac{\pi}{2} + \varphi_0(\beta, s, G) \\
 \sigma &= \frac{\pi}{2} - \varphi_0(\beta, s, G)
 \end{aligned}
 \tag{24}$$

$$\dot{\omega} = \Delta_\omega, \quad \dot{\beta} = \Delta_\beta, \quad \dot{s} = \Delta_s
 \tag{25}$$

where $U = (\Delta_\omega, \Delta_\beta, \Delta_s)$ is vector of the plant inputs as differential corrective actions (integrator inputs), $X = (\omega, \beta, s)$ is vector of dynamical states of the plant, and $Y = (W, \delta, \sigma)$ is vector of outputs. The first harmonic approximation functions A , B and φ_0 are defined in (22). The resonant tank impedance Z is defined by (13). The voltage ratio G is assumed external model parameter: $G =$ or slowly varying in case of stiff loads (like battery), or specific load model can be hooked up to this model by using G as state variable.

The output control problem is formulated as

$$\begin{aligned}
 W &= W_{ref} \\
 \delta &= 0 \\
 \sigma &\geq \sigma_{min}
 \end{aligned}
 \tag{26}$$

where W_{ref} is desired (reference) output transconductance, i.e. output current normalized to input voltage.

Additional optimality condition for state s should be imposed:

$$s \rightarrow \min
 \tag{27}$$

which minimizes the tank current by minimal amount of secondary side shorting (boosting). A mode with $s=0$ corresponds to the buck mode and is essentially a LLC converter (fully driven on primary side and with synchronous rectification on secondary side).

Since commutation parameters are physical quantities, interval constraints are imposed for all state variables:

$$\begin{aligned} \omega_{min} &\leq \omega \leq \omega_{max} \\ 0 &\leq \beta \leq \pi \\ 0 &\leq s \leq \pi \end{aligned} \tag{28}$$

9. Comparison with measured data

In order to validate propose model, the frequency (period T) and voltage ratio G sweep was performed using a hardware prototype of the converter. The input voltage was fixed $V_{in}=64$ V and converter was loaded to constant voltage load. The resonant tank parameters are: $C=8.2$ nF and $L=31$ uH. Transformer turns ratio is 2.2. Model was assuming lossless, i.e. pure LC circuit.

The frequency sweep performed from 700kHz to 380kHz, and voltage ratio inner sweep was from $G=0.4$ to $G=1.3$. Following parameters measured: output current I_{out} along with σ and δ . For the convenience, instead of reporting σ in radians, an equivalent quantity σ/ω in ns was recorded, which is referred as drive phase. The same is for δ : equivalent quantity δ/ω in ns was recorded, which is referred as rectify phase. The measured data then was interpolated between points in 2D plane (frequency and voltage ratio G). For each combination of frequency and voltage ratio G , the switching parameters were found to obtain ZVS on both sides, i.e. hardware was operating in soft switching mode all the time.

The sweep results and comparison with the model are presented in Figures 10, 11 and 12.

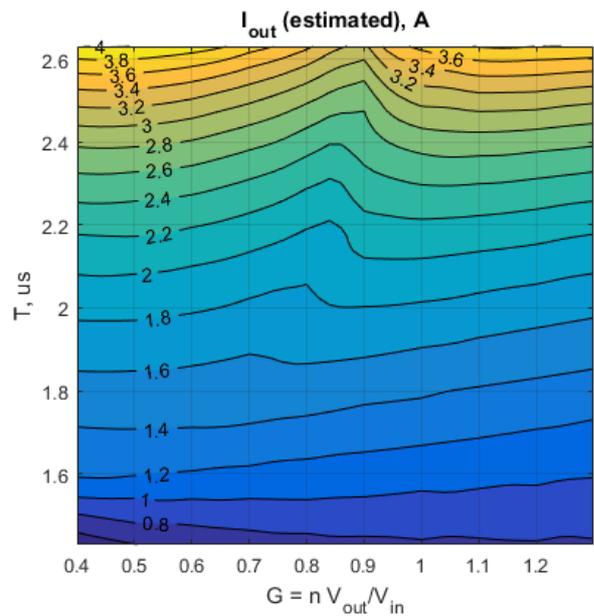
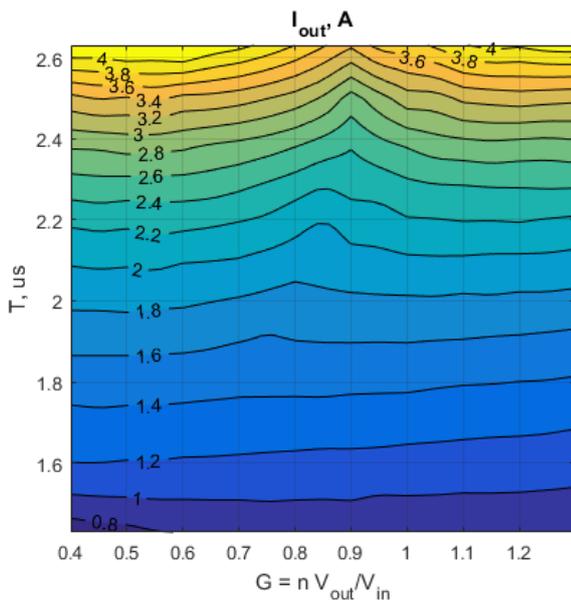


Fig. 10. Measured (top) and calculated by the model (bottom) output current I_{out} .

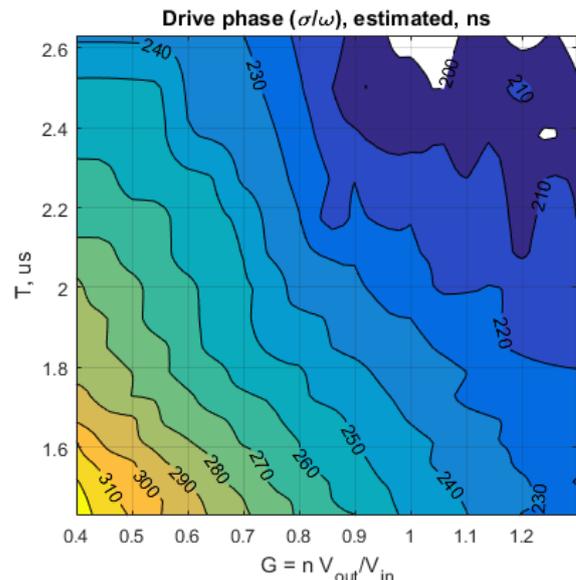
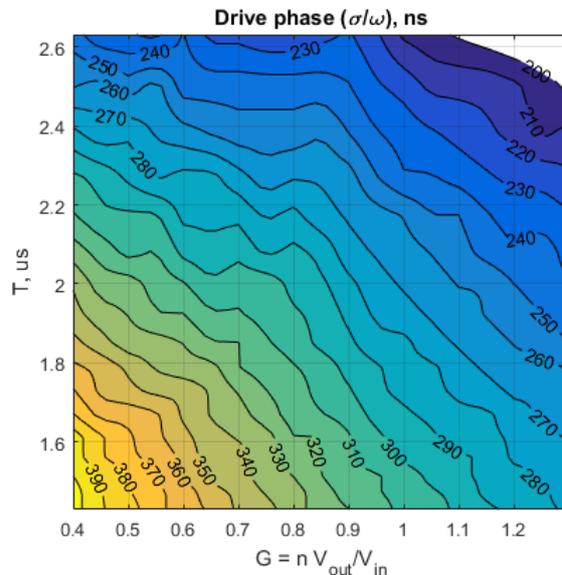


Fig. 11. Measured (top) and calculated by the model (bottom) values of σ/ω .

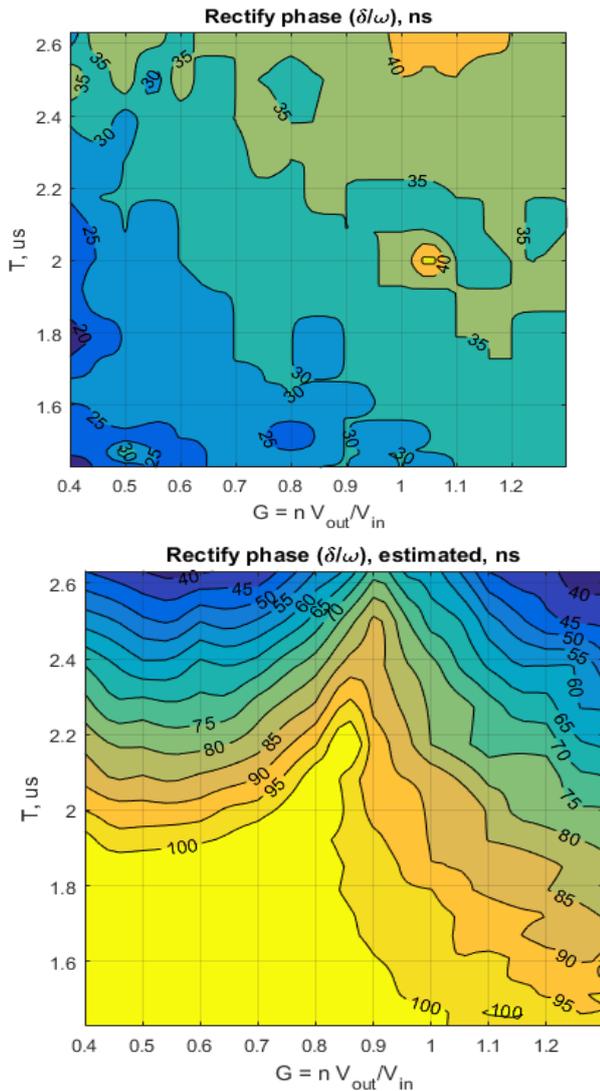


Fig. 12. Measured (top) and calculated by the model (bottom) values of δ/ω .

The output current was varying in boundaries from 0.68A to 4.3A, the difference between calculated by model and measured current ranged between -0.4A to 0.07A. The current is slightly underestimated by the model most of the time. As it seen from the plot, the model correctly predicts a fold of I_{out} surface which happened between buck and boost modes (where s no longer can be 0).

The drive phase (σ/ω) variates in boundaries from 190ns to 405ns, the difference between calculated by model and measured drive phase ranged between -85ns to 12ns. The drive phase is slightly underestimated by the model most of the time.

The rectify phase (δ/ω) was fixed by synchronous rectification and varying very slightly in boundaries from 16ns to 50ns, the difference between calculated by model and measured rectify phase ranged between -4ns to 103ns. The rectify phase is overestimated by the model most of the time.

Although it could seem that model doesn't predict δ/ω in acceptable accuracy, if we will compare the absolute error of prediction to the half period of switching cycle, the resulting relative prediction error is maximum about 10% (Figures 14 and 15). The same result is for estimation of I_{out} : the normalized prediction error to the end of the scale

(maximum current, which is 4.3A) gives also 10% of model accuracy as it demonstrated by Figure 13.

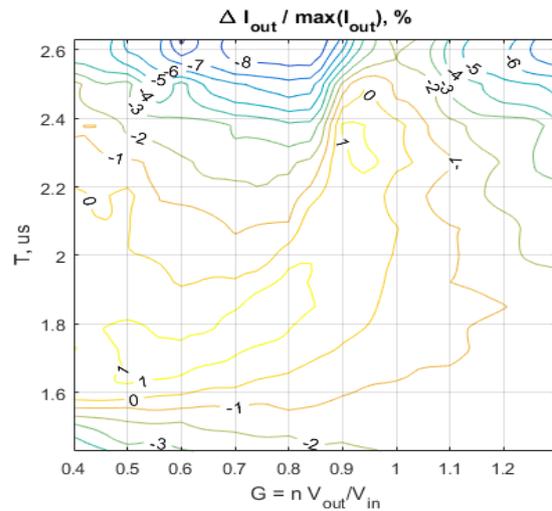


Fig. 13. Estimation error of I_{out} normalized to maximum current achieved during the experiment as $(I_{out}^{est} - I_{out}^{meas}) / \max(I_{out}^{meas})$ by percentage.

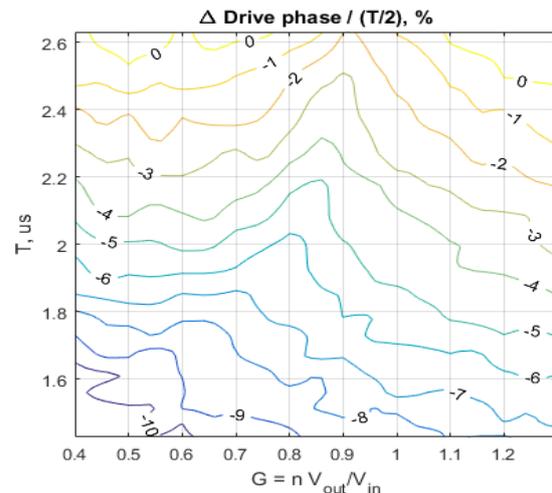


Fig. 14. Estimation error of σ as $2(\sigma^{est} - \sigma^{meas}) / \omega$ by percentage.

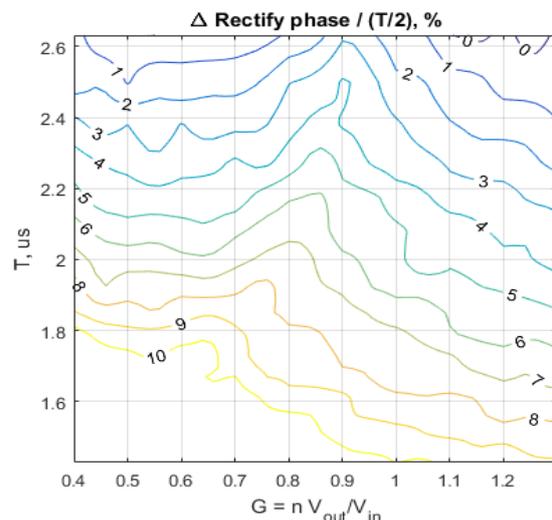


Fig. 15. Estimation error of δ as $2(\delta^{est} - \delta^{meas}) / \omega$ by percentage.

The general conclusion from the data is: the model fairly well predicts the output current, the switching parameters are predicted with about 100ns tolerance. The model is representative for a closed loop control design and analysis in terms of singularity prediction for the output current surface between buck and boost operating modes and the slope of σ/ω . The quantitative verification results are presented in Table 1.

Table 1. The model verification summary.

| | | | |
|--------------------------------|--------|----------|----------|
| Minimum model output value | 0.68 A | 35.7 ns | 194.0 ns |
| Maximum model output value | 4.3 A | 126.1 ns | 324.3 ns |
| Minimum model prediction error | -9.3 % | -0.2 % | -11.2 % |
| Maximum model prediction error | +1.5 % | 14.3 % | 7.8 % |

10. Conclusion

In this paper, the dual-bridge series resonant converter (DB SRC) has been considered in order to obtain its nonlinear state-space model.

The representation of DC/DC converter using voltage sources as bridges with a resonant tank in between has been derived. The switching waveforms in both primary and secondary bridges have been considered and input controls

variables are defined as duty cycles and phase shift for approximated voltages applied to the resonant LC circuit. The turn-on ZVS conditions are quantified as phase shifts of primary and secondary voltage waveforms respect to the moments when resonant tank current becomes zero. The steady-state output current is obtained by first harmonic approximation of a voltage applied to the resonant tank. Then the maximum prediction error of this model is being elaborated by a comparison to the measured data from our hardware prototype, which gives 10% error of output current prediction.

The model obtained can be used for control synthesis for both voltage buck and boost converter operations, which will be addressed in our future publications. Additionally presented model can serve as a real-world benchmark problem for control system design methods, namely feedback linearization, differential flatness, sliding-mode control, etc.

The Simulink model, Matlab scripts and raw data presented in the paper can be downloaded from: <https://sites.google.com/site/akpc806a/ResonantDCDCMode1.zip>

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