Jestr

Journal of Engineering Science and Technology Review 11 (5) (2018) 17 - 25

JOURNAL OF
Engineering Science and Technology Review

Research Article

www.jestr.org

A Comprehensive Time-Domain Analysis of Data Transmission in High Speed Circuits

Sanhaji Houda* **and El Ouazzani Nabih**

Signals, Systems and Components Laboratory (SSCL), EMC unit, Faculty of Sciences and Technology, Fez, Morocco,

Received 4 July 2018; Accepted 4 November 2018

Abstract

In this paper, we present a comprehensive study for analyzing data transmission quality along interconnections taking into account microstrip discontinuities, internal noise sources within active terminations such as Complementary Metal Oxide Semiconductor (CMOS) circuits, and crosstalk. The proposed method consists in combining the Finite Difference Time Domain (FDTD) algorithm to solve Multiconductor Transmission Lines (MTL) equations and the Modified Nodal Analysis (MNA) formulation to include network models of discontinuities, along with the technique of setting eye diagrams. The comparison with Advanced Design System (ADS) software validates the whole simulation process. Several configurations related to bendy interconnections loaded with noisy CMOS circuits have been dealt with. The outcome turned out very useful and can provide valuable information on signal integrity within the sampling context.

Keywords: High speed circuits, Right angle bend, FDTD and MNA methods, Eye Diagram, noisy CMOS.

1. Introduction

Today's emerging high-speed digital applications require the use of more and more sophisticated circuits operating at various frequencies. Improving the efficiency and the accuracy along with reducing power consumption of electronic circuits has always been a bottleneck problem. In addition, the need for circuit miniaturization and low cost application contribute towards more constraints. High speed circuits have also accounted for the occurrence of several damaging phenomena such as crosstalk, interferences, and internal noises [1, 2].

Interconnections, within Printed Circuit Boards (PCB) are amongst the key elements with the most likely potential of bringing out severe disturbances. Geometric discontinuities can take place according to the adopted topologies. Indeed, due to design necessities, interconnection discontinuities such as tees, vias, and bends, usually called passive discontinuities [3] and their effect previously considered insignificant, have now been proven to introduce noticeable signal degradation.

Recently, much attention has been devoted to the analysis of various microstrip discontinuities, and consequently, several methods have been proposed for modeling such a problem. Amongst the most known models, we can find those based on the method of moments [4], the method of lines [5], the analysis with the efficient excess-charge and excess-current techniques [6], the model extraction from the time-domain reflection/transmission (TDR/T) measurement method [7], and the three-dimensional (3-D) transmission-line matrix method [8].

Other harmful phenomena such as interferences, crosstalk and internal noise can occur depending on the frequency range, the design architecture and the load properties.

Knowing the large scale of industrial applications involving CMOS circuits, and the high level of their sensitivity, internal noise must be taken into account in any analysis. Nowadays, designers have come to the conclusion that noise has become even more damaging to data transmission quality, especially at high rates, since active loads have been increasingly employed.

Learning the impact of noise on signal integrity is a very demanding aspect that most of the time is not entirely covered. So, the assumption, previously made, of internal white noise dominance no longer leads to accurate results. On the contrary, designers have to undertake full investigations into the whole phenomenon, which means that the flicker and the thermal internal noises must be included for a large range of frequency. Such a methodology has turned out more important and useful as the simulation process can be carried out in the time domain.

In this paper, interconnections are considered as planar Multiconductor Transmission Lines (MTL), which are governed, under the Transverse-Electromagnetic (TEM) assumption, by the MTL equations with respect to the current and voltage vectors, and the per-unit-length (p.u.l) parameters such as conductance, capacitance, resistance and inductance matrices. The algorithm of the FDTD is easily used for solving these equations in the time domain.

As mentioned above, interconnections' geometric discontinuities, especially bends, can be fully described through lumped elements models. Thus, the MNA formulation facilitates the study of such a problem relying particularly on the inspection matrix.

The originality of this work comes from the combination of the proposed algorithm based on the FDTD and MNA methods, and the technique of setting eye diagrams aiming to investigate the effects of bends, CMOS internal noise and

*E-mail address: sanhaji.houda@gmail.com
ISSN: 1791-2377
doi:10.25103/jestr.115.03

crosstalk on transmission quality at high rates by means of the same code.

2. Circuit topology and properties

2.1. General structure

Due to design constraints and miniaturization, interconnections, within planar circuits, can have several types of discontinuities such as incorporation of lumped elements, non uniform geometrical parameters and presence of bends with various angles [9].

In this study we mainly focus on the most encountered aspect, that is bendy transmission lines' problem as shown in Fig. 1. There is no doubt that bends contribute towards damaging signal integrity. The key aim is to assess the level of degradation compared to the other disturbing parameters by formulating the appropriate circuits' equations with as many bends as possible trough a simple method.

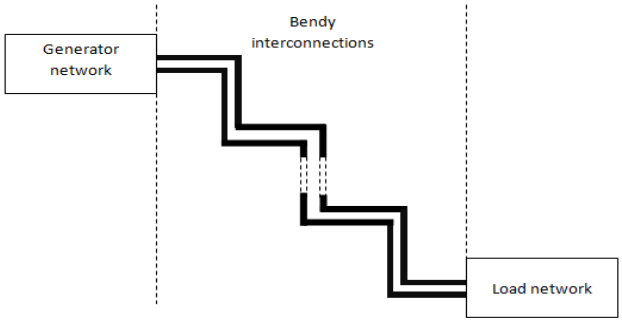
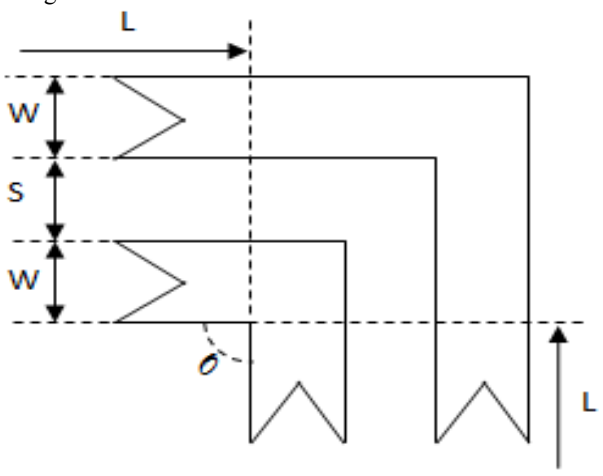


Fig. 1. General structure

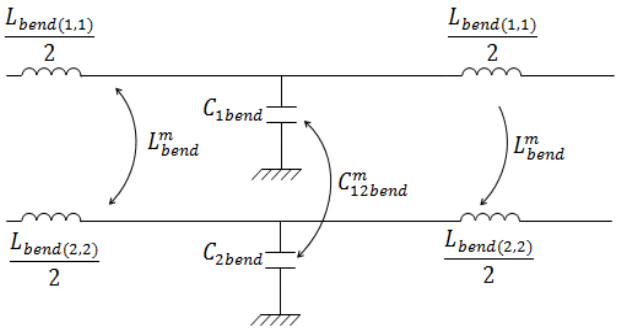
2.2. Bend's equivalent network

Planar circuits are of great interest as far as high speed systems are increasingly employed in many applications. Amongst different configurations available for designs, we have specifically chosen microstrip interconnections with various bends. So, we consider microstrip coupled lines having right angle bends. Fig. 2.a describes the geometric parameters of the discontinuity. According to [6, 8, 10], the developed model can be formed on the basis of the lumped elements network of Fig. 2.b.

The lumped circuit's inductance and capacitance matrices are computed according to the method of [6] and [4], with respect to the dielectric substrate thickness, and the geometric parameters such as the width, the separation and the angle.



(a)

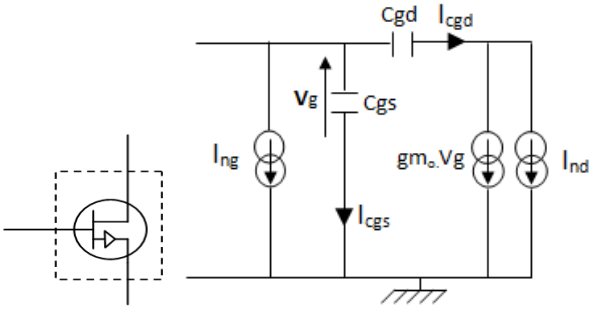


(b)

Fig. 2. Bent coupled transmission lines (a) Physical layout of the bend (b) Equivalent circuit of the bend

2.3. Noise in MOSFET transistors

Numerous components can influence signal integrity within planar circuits. CMOS-based circuits are the most used building blocks and consequently they must be taken into account in the proposed work with respect to their properties. In order to enhance the investigation and have a complete analysis, we deal with microstrip lines loaded with CMOS circuits. So, we include in this study the MOSFET transistor's behavior related to internal noise. The small signal electric model of an NMOS transistor [11], for instance, is described in Fig. 3 where I_{ng} and I_{nd} stand for the gate noise current and the drain noise current, respectively.



(a) (b)

Fig. 3. NMOS Transistor (a) NMOS transistor's model (b) Small signal equivalent circuit of noisy NMOS transistor

Both sources I_{ng} and I_{nd} generate simultaneously thermal and flicker noises depending on the frequency range. Fig. 4 shows that at low frequencies the spectrum is dominated by flicker noise (often denoted as 1/f noise), while at high frequencies the thermal noise is overwhelming. Eq.1 gives the entire description of this aspect:

$$V_i^2(f) = 4KT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K_F}{W_T L_T C_{OX} f} \quad (1)$$

where:

- C_{ox}: gate-capacitance/unit area
- K: Boltzmann's constant = 1.38×10^{-23} JK^{-1}
- T: is the temperature in degrees Kelvin.
- K_F: dependent on device characteristics (Flicker coefficient), varies widely.
- W_T: Transistor's width.
- L_T: Transistor's length.

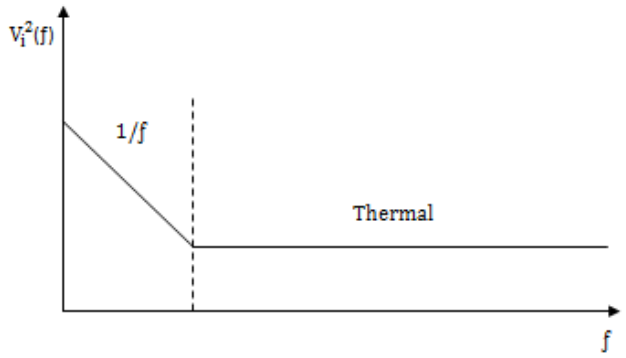


Fig. 4. MOSFET'S noise spectrum

3. Algorithm basic equations

3.1. Circuit Model

As mentioned in section I, the proposed method employs model formulations for both transmission lines and discontinuities. As a matter of fact, interconnections are analyzed through multiconductor transmission lines (MTL) equations and right angle bends are described according to the network of Fig. 2. Thus, Fig. 5 shows the overall circuit under study taking advantage of the flexibility of the proposed models.

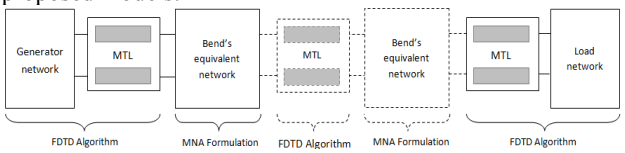


Fig. 5. Model of the circuit

We have chosen the Finite-difference Time-domain (FDTD) algorithm since it is well known to be the most effective numerical method for solving MTL equations of voltages and currents along transmission lines in time and space [10, 12, 13]. The equations describing the interconnecting networks are formulated using the MNA technique that often results in systems, easy to implement algorithmically. There are two main aspects to be considered when choosing algorithms for this purpose: accuracy and speed. The MNA and the 1D-FDTD have been proved to meet these conditions.

3.2. FDTD recursion relations

Let us consider a lossy planar multiconductor transmission line where the wave propagation is described by Eq.2 and Eq.3:

$$\frac{\partial \mathbf{V}(z,t)}{\partial z} = -\boldsymbol{L}\frac{\partial \mathbf{I}(z,t)}{\partial t} - \mathbf{R}\mathbf{I}(z,t) \quad (2)$$

$$\frac{\partial \mathbf{I}(z,t)}{\partial z} = -\mathbf{C}\frac{\partial \mathbf{V}(z,t)}{\partial t} - \mathbf{G}\mathbf{V}(z,t) \quad (3)$$

where $\mathbf{V}(z, t)$ and $\mathbf{I}(z, t)$ are (n × 1) vectors of the line voltages and the line currents, respectively. The position along the line is denoted as z. The line voltages and currents are functions of position z and time t. The per-unit-length parameter ($n \times n$) matrices are **L** (inductance), **C** (capacitance), **R** (resistance), and **G** (conductance).

In order to discretize the equations, we divide the line into NDZ sections each of length Δz. Similarly, we divide the total solution time into NDT segments of length Δt. Each voltage and adjacent current solution points are separated by Δz/2. In addition, the time points are also interlaced, and each voltage time point and adjacent current time point are separated by Δt/2 [14], as shown Fig. 6:

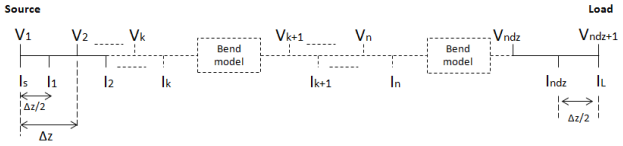


Fig. 6. Spatial discretization of the line

To ensure the stability, the Courant-Friedrichs-Lewy (CFL) condition must be met [15, 16]; that is:

$$\Delta t \leq \frac{\Delta z}{v_p} \quad (4)$$

where v_p is the maximum velocity of the wave propagation.

Now that the voltage and current points have been defined, we develop Eq.2 and Eq.3 according to the FDTD algorithm [2]. So we obtain:

$$\frac{1}{\Delta z}\left(\mathbf{V}_{k+1}^{n+1} - \mathbf{V}_k^{n+1}\right) = -\frac{\boldsymbol{L}}{\Delta t}\left(\mathbf{I}_k^{n+\frac{3}{2}} - \mathbf{I}_k^{n+\frac{1}{2}}\right) - \frac{\boldsymbol{R}}{2}\left(\mathbf{I}_k^{n+\frac{3}{2}} + \mathbf{I}_k^{n+\frac{1}{2}}\right) \quad (5)$$

$$\frac{1}{\Delta z}\left(\mathbf{I}_k^{n+\frac{1}{2}} - \mathbf{I}_{k-1}^{n+\frac{1}{2}}\right) = -\frac{\mathbf{C}}{\Delta t\left(\mathbf{V}_k^{n+1} - \mathbf{V}_k^{n}\right)} - \frac{\boldsymbol{G}}{2}\left(\mathbf{V}_k^{n+1} + \mathbf{V}_k^{n}\right) \quad (6)$$

In order to make the programming process as simple as possible, the required recursion relations become:

$$\mathbf{V}_k^{n+1} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left[\mathbf{V}_k^{n}\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2}\right) - \frac{1}{\Delta z}\left(\mathbf{I}_k^{n+\frac{1}{2}} - \mathbf{I}_{k-1}^{n+\frac{1}{2}}\right)\right] \quad (7)$$

$$\mathbf{I}_k^{n+\frac{3}{2}} = \left(\frac{\mathbf{L}}{\Delta t} + \frac{\mathbf{R}}{2}\right)^{-1}\left[\mathbf{I}_k^{n+\frac{1}{2}}\left(\frac{\mathbf{L}}{\Delta t} - \frac{\mathbf{R}}{2}\right) - \frac{1}{\Delta Z}\left(\mathbf{V}_{k+1}^{n+1} - \mathbf{V}_k^{n+1}\right)\right] \quad (8)$$

where we denote:

$$\mathbf{V}_k^n = \mathbf{V}[(k-1)\,\Delta z, n\Delta t] \quad (9\,a)$$

$$\mathbf{I}_k^n = \mathbf{V}[(k-1/2)\,\Delta z, n\Delta t] \quad (9\,b)$$

3.3. Junction model equations

Formulating circuit equations is usually of great importance to computer-aided analysis in terms of flexibility and time consuming. In order to work towards this aim, the proposed simulation process consists in coupling the MTL equations, solved by the FDTD algorithm, to the MNA technique related to the bends' model. As a result, the junction network involves the right angle bend model and the halves of the MTL's T-cells as shown in Fig. 7.

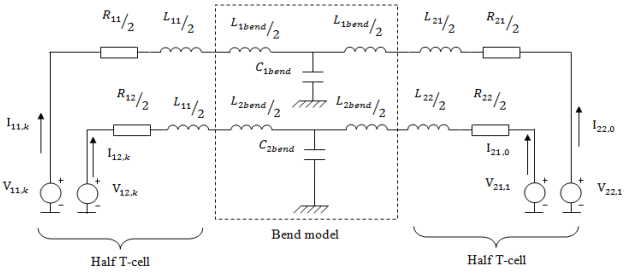


Fig. 7. Junction model of two 2-conductor lines via a bend

The network is governed by the following equation, expressed in s-domain as proposed in [10]:

$$\mathbf{Y}(s) * \mathbf{X}(s) = \mathbf{W}(s) \quad (10)$$

where $\mathbf{Y}(s)$ represents the modified nodal admittance matrix, $\mathbf{X}(s)$ is the unknown vector which includes the nodal voltages and the branch currents $V_{11,km}$, $V_{21,1}$, $V_{12,km}$, $V_{22,1}$, $I_{11,km}$, $I_{21,0}$, $I_{12,km}$, $I_{22,0}$. They are introduced by the additional constitutive relations for the branches that contain voltage sources or current controlled elements. $\mathbf{W}(s)$ includes the values of voltage sources, that are $V_{11,km}$, $V_{21,1}$, $V_{12,km}$, $V_{22,1}$. They are computed through the FDTD algorithm applied to the line equations.

In the time domain, the elements of the modified nodal matrix **Y** can be stored in two constant matrices:

- Matrix **D** that includes the values of **Y** which are not coefficients of partial derivative terms in the network equations.
- Matrix **E** that includes the values of **Y** which are coefficients of partial derivative in the network equations.

$$\mathbf{D}\,\mathbf{X}(t) + \mathbf{E}\,\frac{d\mathbf{X}(t)}{dt} = \mathbf{W}(t) \quad (11)$$

Developing Eq.11 we obtain:

$$\left(\mathbf{D} + \frac{1}{\Delta t}\mathbf{E}\right)\mathbf{X}^{n+1} = \frac{1}{\Delta t}\mathbf{E}\,\mathbf{X}^{n} + \mathbf{W}^{n+1} \quad (12)$$

And the explicit update equation can be written as:

$$\mathbf{X}^{n+1} = \left(\mathbf{D} + \frac{1}{\Delta t}\mathbf{E}\right)^{-1}\frac{1}{\Delta t}\mathbf{E}\,\mathbf{X}^{n} + \left(\mathbf{D} + \frac{1}{\Delta t}\mathbf{E}\right)^{-1}\mathbf{W}^{n+1} \quad (13)$$

3.4. Input voltage

We solve the boundary conditions by using the general voltage FDTD recursion equation and the source constraint at the input termination node:

$$\boldsymbol{k = 1}\,; \quad \mathbf{V}_1^n = \mathbf{V}_s^n - \mathbf{R}_s\mathbf{I}_s^n$$

we have then:

$$\mathbf{I}_s^n = \frac{\mathbf{V}_s^n - \mathbf{V}_1^n}{\mathbf{R}_s}$$

with $\mathbf{R}_s$ is the source resistance matrix.

Substituting the source equation into Eq.7, the voltage at the input is of the form:

$$\mathbf{V}_1^{n+1} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left[\mathbf{V}_1^n\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2}\right) - \frac{2}{\Delta Z}\left(\mathbf{I}_1^{n+\frac{1}{2}} - \mathbf{I}_s^{n+\frac{1}{2}}\right)\right] \quad (14)$$

I_1 and I_s are separated by $\frac{\Delta z}{2}$ as shown in Fig. 6.

Assuming that:

$$\mathbf{I}_s^{n+\frac{1}{2}} = \frac{\mathbf{I}_s^{n+1} + \mathbf{I}_s^{n}}{2}$$

the final expression of the voltage at the input is then:

$$\mathbf{V}_1^{n+1} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2} - \frac{1}{\Delta z}\,\mathbf{R}_s^{-1}\right)^{-1}\left[\mathbf{V}_1^n\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2} - \frac{1}{\Delta Z}\,\mathbf{R}_s^{-1}\right) - \frac{2}{\Delta Z}\,\mathbf{I}_1^{n+\frac{1}{2}} + \frac{1}{\Delta Z}\,\mathbf{R}_s^{-1}(\mathbf{V}_s^n + \mathbf{V}_s^{n+1})\right] \quad (15)$$

3.5. Load voltage

In this case we assume that we have an MTL terminated with noisy CMOS circuits. The circuit of Fig. 8 is taken as an illustrating example. Fig. 9 presents the last cell of the discritized line taking into account the fact that the current and voltage nodes are located at the same point. The loads are connected to the voltage node (NDZ+1).

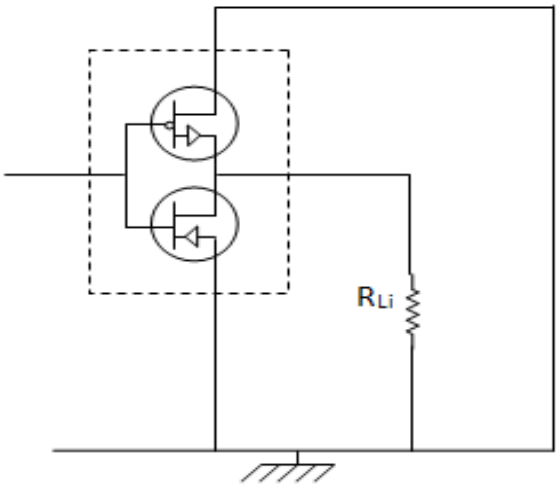


Fig. 8. Considered example of CMOS circuit

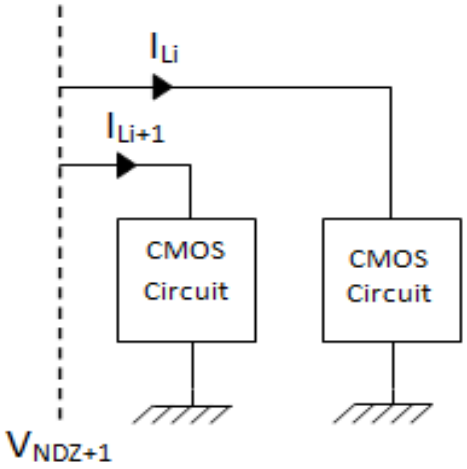


Fig. 9. CMOS-based loads

The MOSFET transistors are modeled by means of the small signal electric network, in which we have inserted internal noise sources I_{ng} and I_{nd} according to the physical phenomenon. Fig. 10 gives the necessary details of the model where "i" denotes the ith conductor of the line.

$\mathbf{I}_L(t)$ at the output of the line is given by:

$$\mathbf{I}_L(t) = \mathbf{I}_{L1}(t) + \mathbf{I}_{L2}(t) \quad (16)$$

Where

$$\mathbf{I}_{L1}(t) = \mathbf{I}_{cgs1}(t) + \mathbf{I}_{ng1}(t) + \mathbf{I}_{cgd1}(t) \quad (17)$$

$$\mathbf{I}_{L2}(t) = \mathbf{I}_{cgs2}(t) + \mathbf{I}_{ng2}(t) + \mathbf{I}_{cgd2}(t) \quad (18)$$

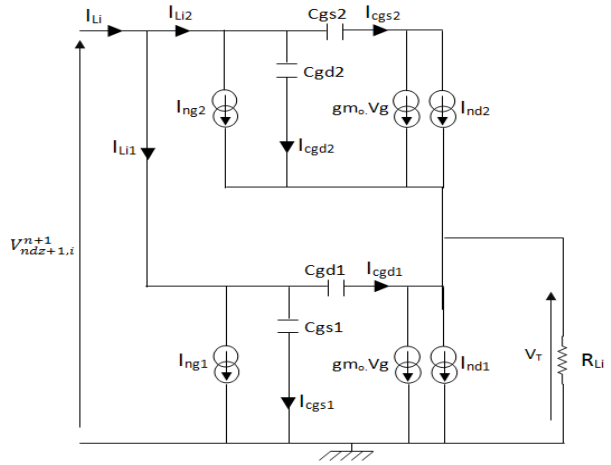


Fig. 10. Noisy CMOS circuit's equivalent model

As shown in Fig. 10, the ($n \times 1$) resulting current vector Developing current terms yields:

$$\mathbf{I_{L1}}(t) = \mathbf{C_{gs1}}\frac{\mathbf{dV_{ndz+1}}(t)}{dt} + \mathbf{C_{gd1}}\left[\frac{\mathbf{dV_{ndz+1}}(t)}{dt} - \frac{\mathbf{dV_T}(t)}{dt}\right] + \mathbf{I_{ng1}}(t) \quad (19)$$

$$\mathbf{I_{L2}}(t) = \mathbf{C_{gd2}}\frac{\mathbf{dV_{ndz+1}}(t)}{dt} + \mathbf{C_{gs2}}\left[\frac{\mathbf{dV_{ndz+1}}(t)}{dt} - \frac{\mathbf{dV_T}(t)}{dt}\right] + \mathbf{I_{ng2}}(t) \quad (20)$$

Applying the FDTD discretization, we obtain:

$$\mathbf{I}_{L1}^{n+1} = \mathbf{C_{gs1}}\frac{\mathbf{V}_{ndz+1}^{n+1} - \mathbf{V}_{ndz+1}^{n}}{\Delta t} + \mathbf{C_{gd1}}\left[\frac{\mathbf{V}_{ndz+1}^{n+1} - \mathbf{V}_{ndz+1}^{n}}{\Delta t} - \frac{\mathbf{V}_T^{n+1} - \mathbf{V}_T^{n}}{\Delta t}\right] + \mathbf{I}_{ng\,1}^{n+1} \quad (21)$$

$$\mathbf{I}_{L2}^{n+1} = \mathbf{C_{gd2}}\frac{\mathbf{V}_{ndz+1}^{n+1} - \mathbf{V}_{ndz+1}^{n}}{\Delta t} + \mathbf{C_{gs2}}\left[\frac{\mathbf{V}_{ndz+1}^{n+1} - \mathbf{V}_{ndz+1}^{n}}{\Delta t} - \frac{\mathbf{V}_T^{n+1} - \mathbf{V}_T^{n}}{\Delta t}\right] + \mathbf{I_{ng2}}^{n+1} \quad (22)$$

The output voltage is expressed with respect to the current, and is written as follows:

$$\mathbf{V}_{ndz+1}^{n+1} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left[\mathbf{V}_{ndz+1}^{n}\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2}\right) - \frac{\mathbf{I}_L^{n+1} + \mathbf{I}_L^{n}}{\Delta z} + \frac{2}{\Delta z}\mathbf{I}_{ndz+1}^{n+\frac{1}{2}}\right] \quad (23)$$

Eq.24 is obtained by inserting the expressions of $\mathbf{I}_L^n$ and $\mathbf{I}_L^{n+1}$ into Eq. 23:

$$\mathbf{V}_{ndz+1}^{n+1} = \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left[\mathbf{V}_{ndz+1}^{n}\left(\frac{\mathbf{C}}{\Delta t} - \frac{\mathbf{G}}{2}\right) + \frac{2}{\Delta z}\mathbf{I}_{ndz+1}^{n+\frac{1}{2}} - \frac{1}{\Delta z}\left(\mathbf{I_{ng1}} + \mathbf{I_{ng2}} + \left(\mathbf{C_{gs1}} + \mathbf{C_{gs2}} + \mathbf{C_{gd1}} + \mathbf{C_{gd2}}\right)\left(\frac{\mathbf{V}_{ndz+1}^{n+1} - \mathbf{V}_{ndz+1}^{n-1}}{\Delta t}\right) - \left(\mathbf{C_{gd1}} + \mathbf{C_{gd2}}\right)\left(\frac{\mathbf{V}_T^{n+1} - \mathbf{V}_T^{n-1}}{\Delta t}\right)\right)\right] \quad (24)$$

Considering the fact that we have two unknown terms, we need to solve the following equation:

$$\mathbf{V}_T^{n+1} = \mathbf{R_L}\,\mathbf{I}_L^{n+1} = \left(1 + \left(\frac{\mathbf{C_{gd1}} + \mathbf{C_{gd1}}}{\Delta t}\right)\mathbf{R_L}\right)^{-1}\left(\mathbf{V}_{ndz+1}^{n+1} - \mathbf{V}_{ndz+1}^{n} + \mathbf{V}_T^{n}\right)\left(\frac{\mathbf{C_{gd1}} + \mathbf{C_{gd1}}}{\Delta t}\right)\mathbf{R_L} \quad (25)$$

where $\mathbf{R_L}$ is an ($n \times 1$) vector representing all the R_{Li} resistors.

The final expressions of $\mathbf{V}_{ndz+1}^{n+1}$ and $\mathbf{V}_T^{n+1}$ are:

$$\mathbf{V}_{ndz+1}^{n+1} = (1 - \mathbf{A'}.\mathbf{B}.\mathbf{B'^{-1}})^{-1}(\mathbf{E} - \mathbf{E'}.\mathbf{B}.\mathbf{B'^{-1}}) \quad (26)$$

and

$$\mathbf{V}_T^{n+1} = (\mathbf{E} - \mathbf{E'}.\mathbf{A'^{-1}})^{-1}(\mathbf{B} - \mathbf{B'}.\mathbf{A'^{-1}}) \quad (27)$$

where:

$$\mathbf{B} = \left(-\left(1 + \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left(\frac{\mathbf{C_{gs1}} + \mathbf{C_{gd1}} + \mathbf{C_{gs2}} + \mathbf{C_{gd2}}}{\Delta t\,\Delta z}\right)\right)^{-1}\left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left(\frac{\mathbf{C_{gd1}} + \mathbf{C_{gd2}}}{\Delta t\,\Delta z}\right)\right)$$

$$\mathbf{E} = \left(\left(1 + \left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\left(\frac{\mathbf{C_{gs1}} + \mathbf{C_{gd1}} + \mathbf{C_{gs2}} + \mathbf{C_{gd2}}}{\Delta t\,\Delta z}\right)\right)^{-1}\left(\frac{\mathbf{C}}{\Delta t} + \frac{\mathbf{G}}{2}\right)^{-1}\right)\left(\mathbf{V}_{ndz+1}^{n}\,\mathbf{B} + \frac{2}{\Delta z}\mathbf{I}_{ndz+1}^{n+\frac{1}{2}} + \frac{1}{\Delta z}\left(\mathbf{I}_{ng1} + \mathbf{I}_{ng2} + \left(\mathbf{C_{gs1}} + \mathbf{C_{gd1}} + \mathbf{C_{gs2}} + \mathbf{C_{gd2}}\right)\left(\frac{\mathbf{V}_{ndz+1}^{n-1}}{\Delta t}\right) - \left(\mathbf{C_{gd1}} + \mathbf{C_{gd2}}\right)\left(\frac{\mathbf{V}_T^{n-1}}{\Delta t}\right)\right)\right)$$

$$\mathbf{A'} = -\frac{\mathbf{C_{gd1}} + \mathbf{C_{gd2}}}{\Delta t}\,\mathbf{R_L}$$

$$\mathbf{B'} = 1 + \frac{\mathbf{C_{gd1}} + \mathbf{C_{gd2}}}{\Delta t}\,\mathbf{R_L}$$

$$\mathbf{E'} = \frac{\mathbf{C_{gd1}} + \mathbf{C_{gd2}}}{\Delta t}\,\mathbf{R_L}\left(\left(\mathbf{V}_T^{n} - \mathbf{V}_{ndz+1}^{n}\right) + \mathbf{I}_{ng}{}^{n} + \mathbf{I}_{nd}{}^{n} + g_{m0}\mathbf{V}_{ndz+1}^{n}\right)$$

The implemented code is then made out of the combination of Eq. 7, Eq. 8, Eq. 13, Eq. 15, Eq. 26, and Eq. 27.

Finally, the resulting voltage values are introduced into a built-in function as input parameters. The programming code's function produces the eye pattern indicating especially the width and the height.

4. Two–bend microstrip line loaded with resistors

4.1. Circuit under study

As a first step, we handle the microstrip circuit presented in Fig. 11 with the substrate dielectric of constant ε_r = 4.5 and of height h = 20 µm. The two main conductors have two right angle bends and are terminated with resistive loads. The geometric parameters of the conductors are: width w = 20µm, separation s = 20µm and total length ℓ = 10cm.

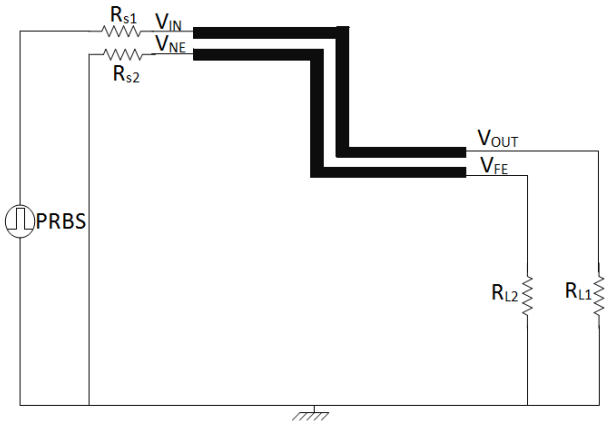


Fig. 11. Circuit with resistive loads

Knowing these parameters, the per-unit-length inductance and capacitance matrices of the circuit are computed according to the method of [13]. So, we obtain:

$$\boldsymbol{C_{Line}} = \begin{bmatrix} 54.80 & -22.11 \\ -22.11 & 54.80 \end{bmatrix} \text{pF/m}$$

$$\boldsymbol{L_{Line}} = \begin{bmatrix} 0.731 & 0.332 \\ 0.332 & 0.731 \end{bmatrix} \mu\text{H/m}$$

On the basis of the bend's model, shown in Fig. 2, and according to the method developed by [4] and [6], the corresponding parameters are computed:

$$\boldsymbol{C_{bend}} = \begin{bmatrix} 0.27 & 0.135 \\ 0.135 & 0.27 \end{bmatrix} \text{pF}$$

$$\boldsymbol{L_{bend}} = \begin{bmatrix} 2.927 & -0.365 \\ -0.365 & 2.927 \end{bmatrix} \text{nH}$$

Furthermore, the MNA vectors and matrices, required for calculating the unknown currents and voltages are as follows:

$$\mathbf{W}(t)=\left[0\ 0\ 0\ 0\ V_{11,\frac{ndz}{2}}(t)\ 0\ 0\ V_{21,\frac{ndz}{2}+1}(t)\ V_{12,\frac{ndz}{2}}(t)\ 0\ 0\ V_{22,\frac{ndz}{2}+1}(t)\ 0\ 0\right]^T$$

$$\mathbf{X}(t) = [V_{N1}\ \ V_{N2}\ \ V_{N3}\ \ V_{N4}\ \ I_1\ \ I_{L1}\ \ I_{L2}\ \ I_2\ \ I_3\ \ I_{L3}\ \ I_{L4}\ \ I_4\ \ V_{C1}\ \ V_{C2}]^T$$

$$\mathbf{D} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \end{bmatrix}$$

and

$$\mathbf{E} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{L_{11}}{2}+L_b & 0 & 0 & 0 & -\frac{L_m}{2}+L_b & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{L_{12}}{2}+L_b & 0 & 0 & 0 & -\frac{L_m}{2}+L_b & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{L_m}{2}+L_b & 0 & 0 & 0 & -\frac{L_{21}}{2}+L_b & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{L_m}{2}+L_b & 0 & 0 & 0 & -\frac{L_{22}}{2}+L_b & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_b & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_b \end{bmatrix}$$

Finally, the source and load resistances are chosen as R_s = R_L = 136Ω and the voltage source is a Pseudo Random Binary Sequence (PRBS) rising to a level of 1V, with a rise time of 0.25ns and a rate of 1Gbits/s. The FDTD – based simulation parameters are: Δz = 1 mm, Δt = 1ps, NDZ =100. We should point out that the whole simulation process produces the $\mathbf{V}_{\boldsymbol{ndz+1}}^{\boldsymbol{n+1}}$ vector that is made of V_{out} and V_{FE}:

$$\mathbf{V}_{ndz+1}^{n+1} = \begin{bmatrix} V_{ndz+1,1}^{n+1} \\ V_{ndz+1,2}^{n+1} \end{bmatrix} = \begin{bmatrix} V_{out} \\ V_{FE} \end{bmatrix} \quad (28)$$

where V_{out} is the voltage at the end of the powered conductor, and V_{FE} represents the far end crosstalk voltage.

4.2. Comparison and validation

Fig. 12 shows the output voltages resulting from both the proposed method and the ADS circuit simulator.

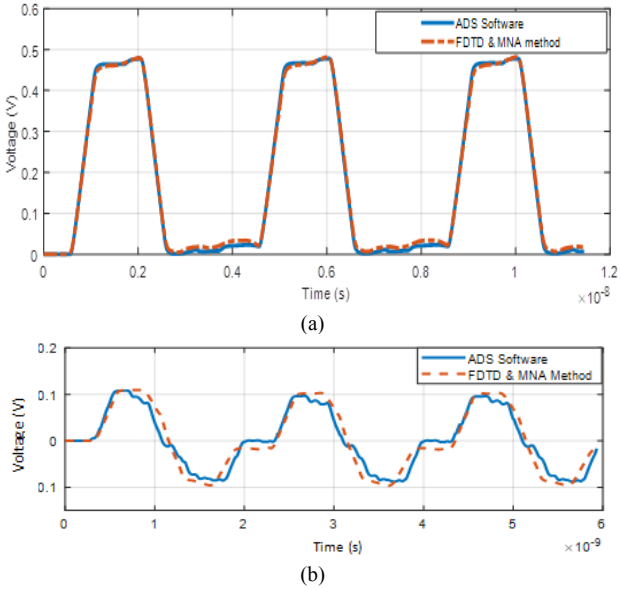


Fig. 12. (a) V_{out} voltage (b) V_{FE} voltage

It is obvious that the confrontation of the two output signals shows an excellent level of agreement between both results. Thus, the validity and the accuracy of the proposed simulation method have been demonstrated.

5. Two-bend microstrip line terminated with CMOS circuits

5.1. Circuit configuration

In many practical cases, data transmission along planar interconnections is bound to undergo several deteriorating phenomena. The aim in this section is to address this issue by dealing with an example that takes into account bends, internal noise and crosstalk Fig. 13. So, we are interested in a Printed Circuit Board (PCB) incorporating a 2-bend lossless microstrip line loaded with two CMOS circuits [17, 18, 19]. The MOSFET transistors involved are assumed to be noisy.

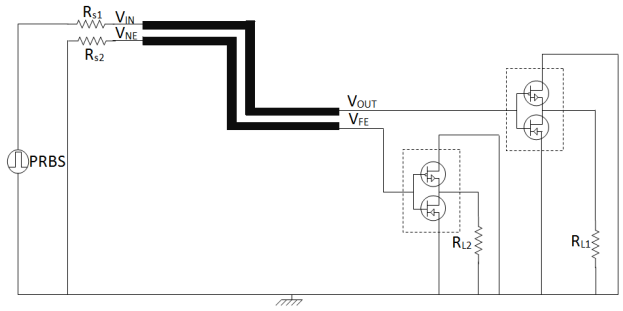


Fig. 13. Circuit under study

The physical and geometric parameters are identical to those of the previous case.

The time domain noise synthesis is made available thanks to the algorithm's guidelines shown in the flowchart of Fig. 3 of [17].

The MOSFET noise vector results from the generation of a White Gaussian Noise simulated in the time domain.

In order to have a random sequence as a function of frequency, the white noise signal is transformed into the frequency mode by means of the Fourier Transform. The left half of the spectrum is multiplied by 1/f, so the power spectral density is proportional to the frequency, and the amplitudes are proportional to $1/\sqrt{f}$. The right half of the spectrum is a copy of the left one, except the DC component and Nyquist frequency. In the last step, noise MOSFET is obtained by transforming the whole spectrum into the time domain.

6. Results and Discussion

In order to illustrate the effect of bends on transmitted signals, we have carried out the necessary time-domain simulations related to the same circuit considering both cases with and without bends. In order to illustrate the impact on transmitted data and make the comparison easier, we have first assumed that the transistors are noiseless. Fig. 14 shows the resulting eye diagrams from which we can notice that the opening varies from 0.73V to 0.53V, and from 0.40ns to 0.35ns making it difficult to have good quality transmission.

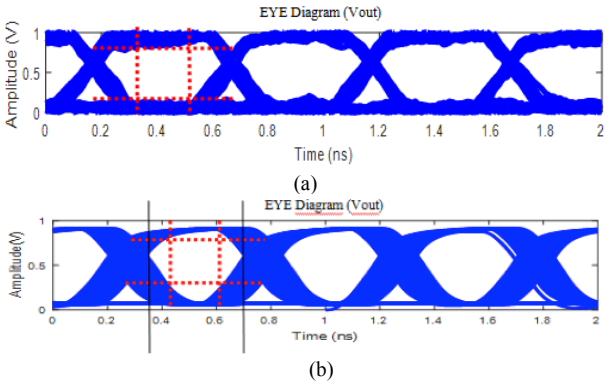


Fig. 14. Eye diagrams of V_{out} (a) MTL connected to noiseless CMOS (b) MTL with two right angle bends connected to noiseless CMOS

In addition to the 2-right angle bends, the transistors' internal noise current sources have now been taken into account. Once again, the eye diagram's width and height in Fig. 15 have become noticeably even more reduced compared to the first case.

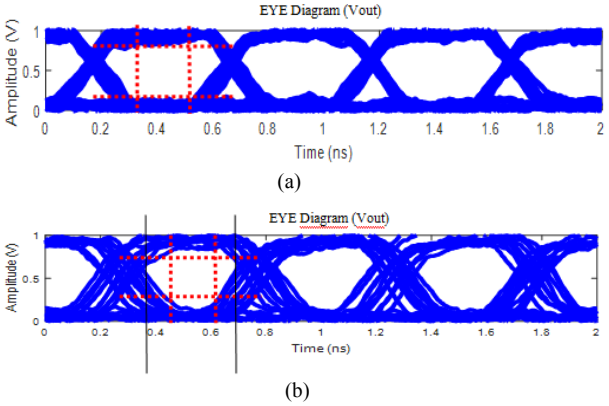


Fig. 15. Eye diagrams of V_{out} (a) MTL connected to noisy CMOS (b) MTL with two right angle bends connected to noisy CMOS

The far end voltage results, shown in Fig. 16, bring out the worst case conditions of data transmission in which bends, noise and crosstalk are all included.

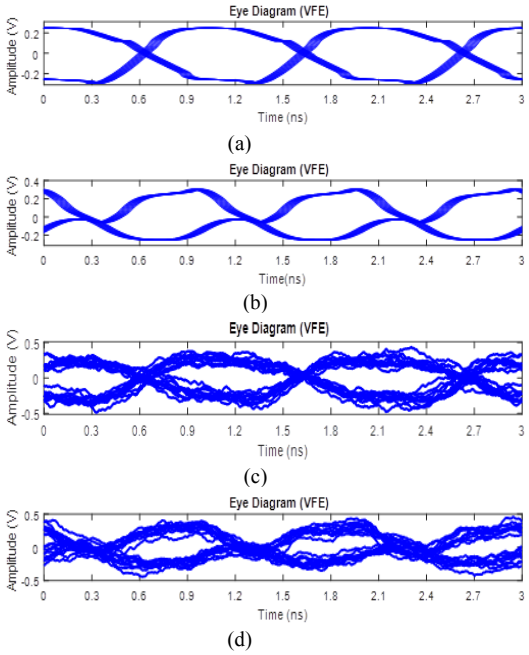


Fig. 16. Eye diagram of V_{FE} (a) MTL connected to noiseless CMOS (b) Bent MTL connected to noiseless CMOS (c) MTL connected to noisy CMOS (d)Bent MTL connected to noisy CMOS

Tab. 1 and Tab. 2 give different values of various eye diagram parameters related to the handles cases.

Table 1. V_{out} Eye Diagram's parameters

	MTL connected to noiseless CMOS	**MTL connected to noisy CMOS**	**Bent MTL connected to noiseless CMOS**	**Bent MTL connected to noisy CMOS**
Eye with (ns)	0.40	0.38	0.35	0.31
Eye height (V)	0.73	0.66	0.53	0.46

Table 2. V_{FE} Eye Diagram's parameters

	MTL connected to noiseless CMOS	**MTL connected to noisy CMOS**	**Bent MTL connected to noiseless CMOS**	**Bent MTL connected to noisy CMOS**
Eye with (ns)	0.51	0.45	0.40	0.31
Eye height (V)	0.45	0.36	0.31	0.24

7. Conclusion

This paper has proposed a time-domain approach completely covering the most important factors that affect data transmission quality such as bends, noise and crosstalk. The simulation process relies mainly on solving MTL equations through the FDTD algorithm. In order to make the whole operation easy and efficient, discontinuities models are included in the developed formulation and then handled by the MNA technique. As an example of typical load, a CMOS circuit has been considered with the emphasis on the internal noise current sources.

The proposed code has first been validated by comparing different resulting voltages with those of the ADS software. More importantly, it has been proven efficient as well as accurate in terms of predicting termination voltages and eye diagram setting. Several simulations have been carried out confirming the significant impact that bends, noise and crosstalk can have on signal integrity and consequently on the whole process of sampling.

References

1. R. D. Silva, I. Gilson. Wirth, Ralf. Brederlow, Novel analytical and numerical approach to modeling low-frequency noise in semiconductor devices, Physica A: Statistical Mechanics and its Applications, **Vol. 362**, No. 2, pp. 277-288, (2006).
2. N. Elouazzani, D. Tahri, H. Kabbaj, Transient analysis of nonuniform transmission lines with skin effect,Annals of telecommunication, **Vol. 54**, No. 5, pp. 331- 340, (1999).
3. F. W. L. Kung and H. T. Chuah, System modeling of high speed digital printed circuit board using spice, Progress In Electromagnetics Research, PIER, **Vol. 20**, pp. 179–211, (1998).
4. A. Hill andV. K. Tripathi, Analysis and modeling of coupled right angle microstrip bend discontinuities, in IEEE MTT-S Int. Microw. Symp. Dig, **Vol. 3**, pp. 1143–1146, (1989).
5. F. J. Schmuckle and R. Pregla, The method of lines for the rigorous full wave analysis of rectangular bends of multiple-line-systems, in IEEE MTT-S Int. Microw. Symp. Dig, **Vol. 2**, pp. 797–800, (1992).
6. P. H. Harms, R. Mittra, Equivalent circuits for multiconductor microstrip bend discontinuities, IEEE Transactions in Microwave Theory and Techniques, **Vol. 41**, No. 1, (1993).
7. J.-M. Jong, B. Janko, and V. Tripathi, Equivalent circuit modeling of interconnects from time-domain measurements, IEEE Trans. Comp. Hybrids, Manuf. Technol, **Vol. 16**, No. 1, pp. 119–126, (1993).
8. C. Boussetta, F. Ndagijimana, and J. Chilo, Modeling of multiconductor microstrip bend discontinuities, Proc. IEEE 3rd Topical Elect. Performance Electron Packag, pp. 148–150, (1994).
9. T. K. Tang, M. S. Nakhla, R. Griffith, Analysis of Lossy Multiconductor Transmission Lines using the Asymptotic Waveform Evaluation Technique, IEEE Transactions On Microwave Theory and Techniques, **Vol. 39**, No. 12, (1991).
10. D. Mardare, J. LoVetri, The Finte-Difference Time-Domain Solution of Lossy MTL Networks with Nonlinear Junctions, IEEE Transaction on Electromagnetic Compatibility, **Vol. 37**, No. 2, (1995).
11. P. Pouvil, Composants semiconducteurs micro-ondes, Elsevier Masson, France, (1994).
12. G. Ngendakumna, N. Elouazzani, Simulation of Ultra-Wideband Miscrostrip Antenna Based on Laguerre-Finite-Difference Time-Domain (LFDTD) Algorithm, IJCSNS International Journal of Computer Science and Network Security, **Vol. 13**, No. 11, pp. 33-44, (2013).

13. M. D. Sullivan, Electromagnetic Simulation Using the FDTD Method, Wiley-IEEE Press, (2000).
14. C. R. Paul, Incorporation of terminal constraints in the FDTD analysis of transmission lines, IEEE Trans. Electromag. Compat, **Vol. 36**, pp. 85-91, (1994).
15. R. C. Paul, Analysis of Multiconductor Transmission Lines, John Wiley and Sons Ltd, (1994).
16. J. A. Roden, R. C. Paul, T .W. Smith, D. s. Gendey, Finite-Difference Time Domain Analysis of Lossy Transmission Lines, IEEE Transactions on electromagnetic compatibility, **Vol. 38**, No. 1, pp. 15-24, (1996).
17. H. Sanhaji, N. El Ouazzani, FDTD-Based Analysis of High Speed Data Transmission Along Interconnections Terminated with Noisy MOSFET, International Journal on Communications Antenna and Propagation (I.Re.C.A.P.), **Vol. 7**, No. 2, (2017).
18. J. S. Kolhatkar , C. Salm , M.J. Knitel , and H. Wallinga, Constant and Switched Bias Low Frequency Noise in p-MOSFETs with Varying Gate Oxide Thickness, European Solid-State Device Research Conference , Bologna, Italy, pp. 83-84, (2002).
19. J. S.Kolhatkar, Steady-state and cyclo-stationary RTS noise in MOSFETS, Twente Univ, Enschede, The Netherlands, (2005).
20. G. B. Robert, Introduction to Random Signal Analysis and applied Kalman Filtering John Wiley and Sons, pp. 3-95, (1983).
21. P. Athanasios, Probability Random Variables and Stochastic Processes, Mcgraw-Hill College, (1991).