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Design of Reversible Combinational Circuits Using New Reversible Logic Gate

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Abstract

In this paper the authors have proposed a new 3×3 reversible gate and also proposed the reversible combinational logic circuits with better optimized quantum cost, garbage outputs and delay. The proposed new reversible logic gate is used to design of reversible 1-bit comparator circuit and realization of different logic functions such as NOT, AND, NAND, OR, NOR, XOR, NXOR. The proposed new reversible logic gate is represented by quantum implementation. The quantum cost of proposed gate is 4. The quantum cost, garbage output and delay of proposed reversible 1-bit comparator circuit are 6 which is better w. r. t. previously reported results.

Keywords: Quantum computing; code converter; reversible logic gate; quantum cost; delay

1. Introduction

The quantum computing is very much promising field of engineering and technology due to low power dissipation, high speed operation. The very essential parameters of the design and implementation for reversible logic circuits are the quantum cost, delay and garbage outputs [1-4]. The quantum cost of a reversible logic gate is the numbers of 1×1, 2×2 quantum gate such as NOT, Controlled-V, Controlled-V^+ and CNOT gates[2, 5-7]. The garbage outputs are the unutilized outputs presents in the reversible circuits. The delay is the maximum number of gates in a path from any input to any output line. Hence, the most important objective in reversible logic design and development is to minimize the quantum cost (QC), garbage outputs (GO) and delay (D) [4-10]. The design of reversible comparator circuits is reported in [11-13].

In this paper we have proposed a new reversible logic gate (NRLG) and also proposed the quantum cost, garbage outputs and delay optimized design of different reversible combinational logic circuit such as 1-bit comparator circuit. The paper is organized as follows, section-2 presents the basic concept of reversible gate, section-3 presents the proposed work, section-4 presents the conclusion.

2. Basic concepts

The reversible logic function is an equal number of input and output logic functions, the reversible gate having same no. of input and output terminals, which can be represented as K×K, where K is the number of input and output. If input vector is (I1, I2,……..Ik) then the output vector is represented by (O1, O2,……Ok). Fig. 1 shows the K×K reversible logic gate. The input and output have one-to-one mapping. This helps to find out the outputs from the inputs and also the inputs can be uniquely recovered from the outputs [3].

There are several reversible gates for example reversible NOT gate, Feynman gate(FG) [7], Peres Gate(PG) [8] etc. but in this paper only reversible NOT gate and proposed NRLG is used.

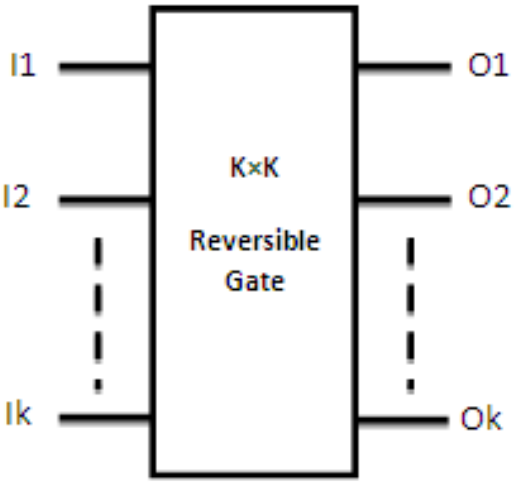

Fig. 1. K×K reversible logic gate.

3. Proposed work

In this section we have describe the new reversible 3×3 NRLG and also describe the QC, GO and D optimized 1-bit comparator circuit using proposed new logic gate.

3.1. Proposed New Reversible Logic Gate (NRLG)

The proposed NRLG has 3 input and 3 output terminals which is shown in Fig. 2. The three inputs are A, B, C and

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three outputs are P=A, Q=(A ⊛ B), R=(AB' ⊛ C). The table I shows the truth table of proposed NRLG. The fig. 3 shows the quantum representation of NRLG.

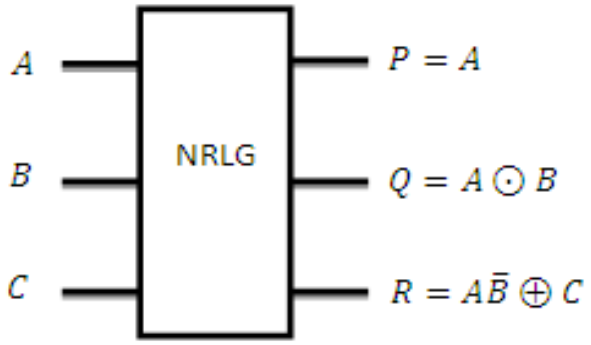

Fig. 2. Proposed 3×3 new reversible logic gate.

The Fig. 4(a) to Fig. 4(h) shows the functional realization of proposed NRLG. In fig. 4(a), A=0 so P=0, Q=B' and R=C. In fig. 4(b), A=1 so P=1, Q=B and R=B⊙C. In fig. 4(c), B=0 so P=A, Q=A' and R=A⊕C. In fig. 4(d), B=1 so P=A, Q=A and R=C. In fig. 4(e) XOR and OR operation can be implemented using NRLG and NOT gate. In fig. 4(f), C=0 so P=A, Q=A⊙B and R=AB', In fig. 4(g) XOR and NAND operation can be implemented using NRLG and NOT gate, In fig. 4(h) XOR and AND operation can be implemented using NRLG and NOT gate.

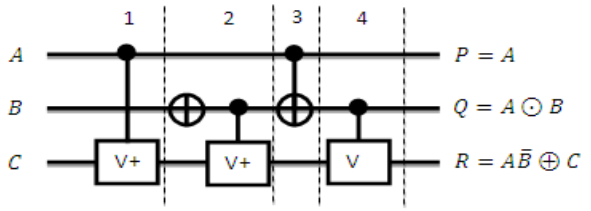

Fig. 3. Quantum representation of proposed NRLG.

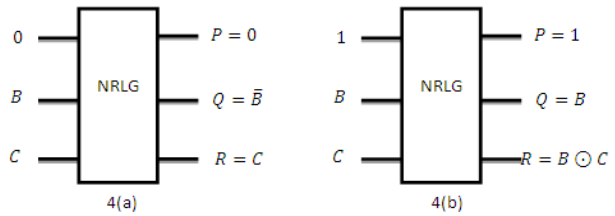

Fig. 4(a) and 4(b). Functional operation of proposed NRLG with A=0 and A=1..

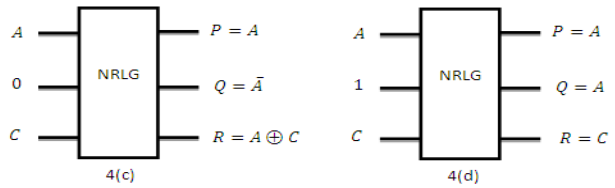

Fig. 4(c) and 4(d). Functional operation of proposed NRLG with B=0 and B=1.

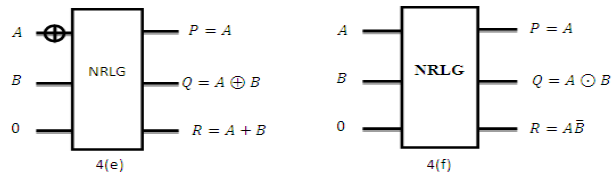

Fig. 4(e) and 4(f). Realization of XOR and OR operation using NRLG.(f) Functional operation of proposed NRLG with C=0.

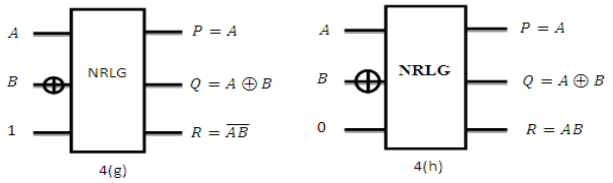

Fig. 4(g) and 4(h). Realization of NAND, AND, XOR operation using proposed NRLG.

Table 1. Truth table of proposed NRLG.

A	B	C		P	Q	R
0	0	0		0	1	0
0	0	1		0	1	1
0	1	0		0	0	0
0	1	1		0	0	1
1	0	0		1	0	1
1	0	1		1	0	0
1	1	0		1	1	0
1	1	1		1	1	1

3.2 Proposed 1 Bit Comparetor Circuit Using NRLG

The proposed 1-bit reversible comparator circuit can be design using one NRLG, two FG, Fig. 6 shows the basic block diagram of proposed circuit. The inputs are A, B and outputs are X(A>B), Y(A=B), Z(A<B). The table IV and table V shows the truth table and comparison result of 1 bit comparator circuit. The QC, GO and D of proposed circuit are correspondingly 6, 1 and 3 which is better than latest reported result [12]. The improvement % of QC, GO and D with respect to latest reported result in [12] is 33.33%, 50% and 0%.

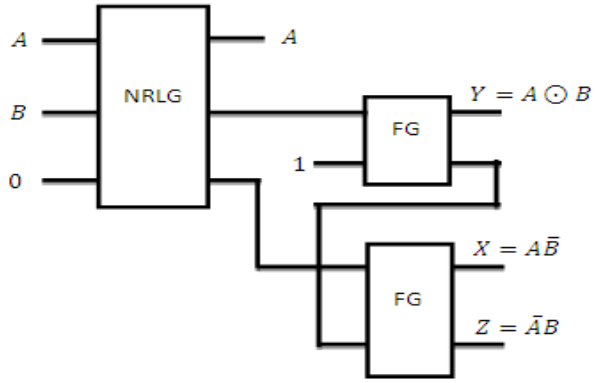

Fig. 6. Block diagram of proposed 1-bit comparator using NRLG.

Table 2. Truth table of 1 bit comparator circuit using proposed NRLG.

A	B		X=A>B	Y=A=B	Z=A<B
0	0		0	1	0
0	1		0	0	1
1	0		1	0	0
1	1		0	1	0

Table 3. Comparison result of 1 bit comparator circuit using proposed NRLG.

	QC	GO	Delay
Proposed design	6	1	3
Ref [12]	9	2	3
Ref [13]	11	1	3
Improvement %	33.33-45.45	0-50	0-25

3.3. Realization of Different Logic Function Using NRLG

The proposed gate can be use to design almost all logic operations. The Fig. 2 to Fig. 4 shows the different logic representation using proposed NRLG such as NOT, AND, NAND, OR, XOR, XNOR etc. In fig. 4(a), NRLG acts as inverter and buffer. In fig. 4(b) NRLG acts as buffer and XNOR gate. In fig. 4(c) NRLG acts inverter and XOR gate. In fig. 4(d) NRLG acts as buffer. In fig. 4(e) NRLG acts as inverter, XOR and OR using NOT gate. In fig. 4(f) C=0 so P=A, Q=A⊙B and R=AB'. In fig. 4(g), NRLG act as buffer, XOR and NAND gate. In fig. 4(h), buffer, XOR and AND are design using NRLG and NOT gate.

4. Conclusions

The authors have proposed the new reversible logic gate (NRLG) and also proposed the quantum cost, garbage outputs and delay optimized different reversible combinational logic circuits using proposed new gate, such as 1-bit comparator circuit. In case of 1 bit comparator circuit the improvement % of QC and GO is 33.33% and 50% with respect to latest reported result in [12]. The proposed design is very useful in quantum computing, cryptography, reversible ALU etc.

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