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Advanced MOSFET Technologies for Next Generation Communication Systems - Perspective and Challenges: A Review

Himangi Sood[1], Viranjay M. Srivastava[2,*] and Ghanshyam Singh[3]

[1]*Department of Electronics and Communication, Jaypee university of Information Technology, Waknaghat, Solan – 173234, India.*
[2]*Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban – 4041, South Africa.*
[3]*Department of Electrical and Electronics Engineering Sciences, Auckland Park Kingsway Campus, University of Johannesburg, PO Box 524, Johannesburg - 2006, South Africa.*

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Abstract

In this review, authors have retrospect the state-of-art dimension scaling and emerging other non-conventional MOSFET structures particularly, the Double-Gate (DG) MOSFET and Cylindrical Surrounding Double-Gate (CSDG) MOSFET. These are presented for the future devices to reduce the short channel effects for the next generation communication system as the dimension of device approaches to the nanometer regime. The discussion on advantages and compact modeling approaches of both the MOSFETs have been presented. Moreover, these compact models are very useful to understand the physical characteristics of devices and also necessary for the circuit simulators, which are presently most growing research areas. Therefore, a review of the various approaches to developing the complete compact models for DG MOSFETs and CSDG MOSFET is necessary. The significant effect that is the short channel effects are also looked upon with the help of reported literatures. In addition to this, with the next generation communication prospective, the DG MOSFETs and CSDG MOSFETs have been discussed, which prove to be advantageous for the Terahertz (THz) frequency regime where high speed data transmission and reduced power consumption are the major requirements.

Keywords: MOSFET, Short channel effects, Scaling techniques, Gate engineering, Double-gate (DG) MOSFET, Surrounding-gate MOSFET, Cylindrical surrounding double-gate (CSDG) MOSFET, Compact model, Leakage current, RF performance, Nanotechnology, VLSI.

1. Introduction

Over the last two decades, it has been observed that after every *18 months* the wireless data rate doubles and is approaching the capacity of wired communication systems as shown in Fig. 1 [1]. In addition to this, till *2020* the data rate is reaching out to be greater than *1 Gbps*. Therefore, to meet the requirement for future wireless network, new technologies are needed which should have high data handling capacity and reduction in overall power consumption of the system. Therefore, the *THz* range of frequency spectrum (from *300 GHz* to *3 THz*) can provide multiple *GHz* channel bandwidths. This spectrum provides the possibility to transmit at high data rate that is multi-gigabits per second. The recent research activities in THz technologies are increasing into much broader applications such as medical imaging, and wireless sensors and communications [2, 3]. *Akyildiz et. al.* [4] have discussed the *THz* band communication and addressed the capacity limitation of the current wireless communication system. Moreover, the other foremost requirements of the next generation communication system are the low power consumption and high processing speed, which should also be met in a much effective way.

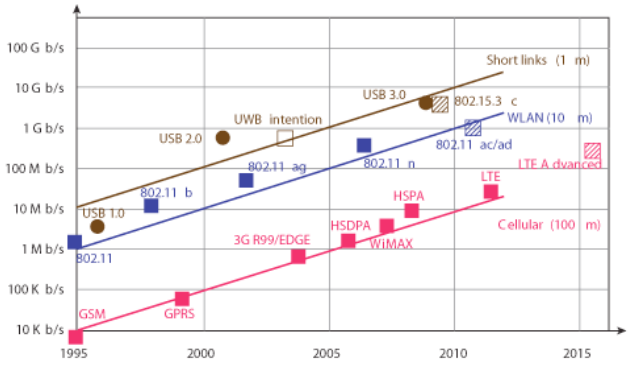

Fig. 1. Edholm's law of data rates [1].

In addition to this, the major key for enabling the effective wireless communication is the Radio Frequency Integrated Circuits (RFIC). The analog components designing at high frequencies adds up to form RFIC design. Moreover, the analog components designing is used at the low frequencies and the high frequency make use of the microwave theory where the concept of the transmission-line is very important [5]. In addition to this, the RF circuitry can be designed by merging various forms of chips and by using the same process as that for the traditional digital or baseband circuitry, otherwise that would be divided into multi-chipsets. However, the single-chip integration also reduces the drawn current by reducing the number of off-chip loads which are necessary to drive multiple, non-integrated chipsets [6]. Single chip integration is a basic

*E-mail address: viranjay@ieee.org
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model of current steering. Means if single chip integration circuit is used, then for the various current sources, only one chip integration is required which gives various current with current steering technology. The consumer's requirements for the RFIC design are the portability, low power consumption, multi-functionality, and miniaturization, which would further combined to reduce the overall cost of the System-On-Chip (SoC). As this is single-chip integration will ease the functionality (due to VLSI and ULSI technology), and low power consumption (due to one power source), and also bulk production will tends to reduction in the production cost.

However, due to reduced energy consumption of the MOSFET, the ultra-fast communication is the better option [7]. Although, the designing of device for high frequency range is a very crucial task, therefore new device structures has to be incorporated into the communication system that would provide the desired performance for the next generation communication system. However, *Fujishima* [8] has demonstrated that how the low-power and high speed communication for THz can be balanced. In addition to this, the MOSFET has been an emerging device for RF/analog communication applications and the demand of the industry is encouraging for the replacement of costly, huge sized, and more power consuming devices with low power and high-density RF devices.

The remaining of the work has been organized as follows. In the Section 2, concise an idea of MOSFET as well as potential tools used for the technology advancement prior to move onto the new device structures of MOSFET and the RFIC design performance parameters in the *THz* range. The scaling procedure for the devices have been analysed in the Section 3. By the scaling, short channel effects ceates which has been analyzed in the Section 4. The Section 5 contains advanced MOSFET structures. The DG MOSFET has been discussed in the Section 6. The extenstion of DG MOSFET know as cylindrical-gate MOSFET has been summarized in the Section 7. The advanced version of MOSEFT which includes DG MOSFET and cylindrical-gate MOSFET known as CSDG MOSFET has been visualized in the Section 8. Finally, Section 9 concludes the work and recommend the future aspets.

2. Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

Initially, the need for smaller, cheaper, faster, less power consuming devices and replacement for the large sized vacuum tube was encouraged in 1930 to give the basic concept for Field Effect Transistor (FET) [9]. However it was unable to demonstrate its structure due to the presence of surface states at the interface of oxide and semiconductor that prevents the electric field from penetrating the semiconductor material. This predicament was overcome by *Kahng and Attala* [10] who invented the insulated gate FET by using the combination of three layers i.e. Metal (M), Oxide (O) and Semiconductor (S). Moreover, the presence of the grown silicon dioxide layer on semiconductor surface reduces the amount of surface states and known as MOSFET.

Several milestones in the bulk technology are summed up by *Wong et. al.* [11] is presented in Table 1 starting from the invention of MOSFET since 1960. The authors [11] have also pointed out the other advancements such as the silicided polysilicon gate to retrograde channel doping and the use of copper interconnect further increases the performance parameters (due to their permittivity and other physical prameters), which increases the drain current and reduces the leakage current of the MOSFET.

Table 1. Milestones in the bulk technology [11].

Year	Technology	Channel Length (μm)
1960	MOSFET	-
1969	Ion-implanted channel	-
1971	Intel 4064 Microprocessor	10
1979	Silicided polysilicon gate	1
1986	Retrograde channel doping	0.5
1993	Copper interconnect	-

Since then, MOSFET is used as a fundamental switching device with four terminals as shown in Fig. 2 (Gate, Drain, Source and Body) in Very Large Scale Integrated (VLSI) circuit that is controlled by the electric field applied to one of the terminal that is a gate. Moreover, the terminals drain, source and gate are highly doped, but the body is lightly doped. The gate electrode is made of metal or poly-silicon and is separated from silicon body with a thin insulating film which acts as energy barrier between the gate electrode and silicon body. The conductive region of the device may either be *p*-type or *n*-type depending upon the application. With the proper bias condition, significant current can flow between the source and drain terminals of the MOSFET which makes the possibility of two types of current flow in the device:

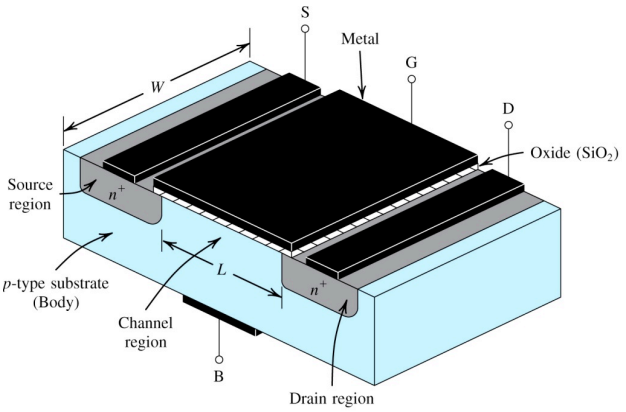


Fig. 2. The four terminals MOSFET Structure [12].

a) *Diffusion current*: when the applied gate voltage is less than the threshold voltage.

b) *Drift current*: when the applied gate voltage is greater than that of the threshold voltage.

On the basis of flow of current between the drain and source, three operating regions are feasible [12-14]:

a) *Cutoff region*: where no current flows excluding sub-threshold current which becomes dominant when the dimensions of the device becomes significantly smaller.

b) *Linear region*: where the linear current flows between the source and drain terminals, and

c) *Saturation region*: where the current gets saturated as the channel formed between the source and drain is pinched-off at the drain side.

3. Scaling Procedure

To improve the system reliability, current drive, computational capability and integration density at significantly lower cost, the scaling should be applied [15]. The basic idea behind the scaling, lies in to producing smaller transistor with performance similar to that of the larger one and simultaneous reduction of all the dimensions [16, 17]. However, the geometrical ratio (the ratio between the horizontal dimensions (channel width) to the vertical dimension (channel length)) should be maintained with precision. Moreover, with the use of scaling, the reduction in delay and further the advancement in clock frequency have been observed. In addition to this, the device density is doubled, and the reduction in energy consumption with active power per transition is also reported in ref. [18]. Fig. 3 shows the linear circuit performance due to the technology scaling.

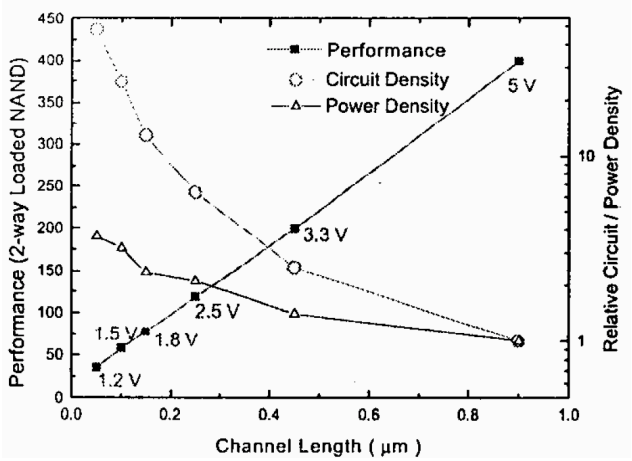
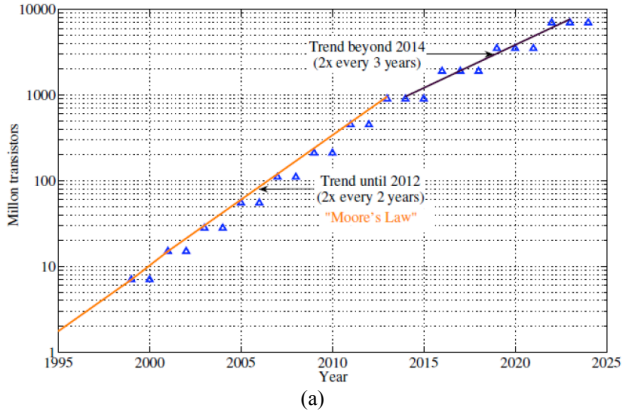
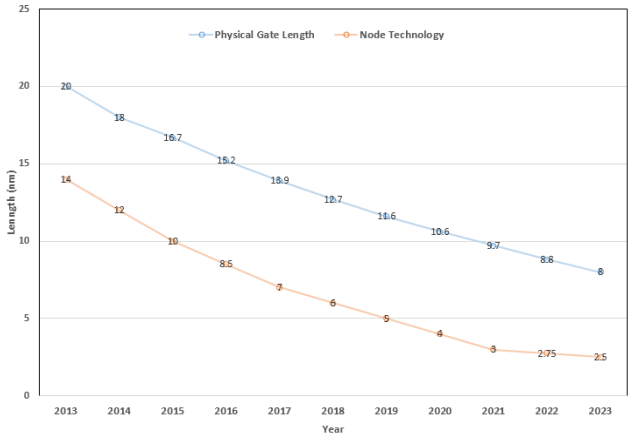


Fig. 3. Trends for CMOS performance, power density and circuit density [18].

Therefore, the semiconductor industries have encouraged to project the scaling theory in addition to the observation made by *Moore's law* [19, 20], in the form of International Technology Roadmap of Semiconductor (ITRS) [21]. Fig. 4(a) forecasts the dimension reduction over the year through the ITRS roadmap, and Fig. 4(b) suggests that upto to *2023*, the doubling of transistors follows the Moore's law. However, after that the pace of advancement (i.e. doubling) will slow down to every *3* years. Fig. 5 suggests the conceptual idea for scaling, where a, W, W_d, L_g and t_{ox}, represents the scaling factor, wiring width, depletion depth, gate length, and oxide thickness, respectively.



(a)



(b)

Fig. 4. (a) Semiconductor technology road map [21], and (b) Technology progress [22].

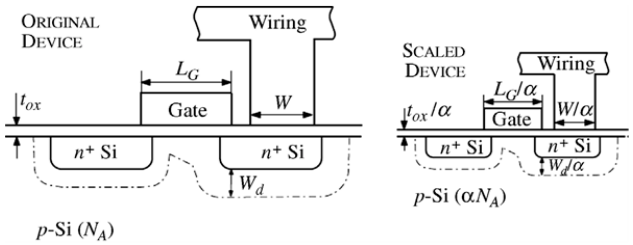


Fig. 5. Schematic diagram of device scaling [17].

However, based on the conceptual idea, the classical scaling techniques are classified into two potential classes such as :

a) *Constant-voltage scaling*: In the constant voltage scaling [23], all the dimensions of device are scaled-down keeping the power supply voltage and terminal voltages unchanged so as to remain compatible to prevailing electronic system regarding supply voltage standards. This scaling technique is not a practical one as the power dissipation increases to a high level, leads to the electro-migration, hot carrier degradation, and oxide breakdown [24].

b) *Constant-field scaling*: The constant field scaling introduced by *Dennard et. al.* [16], all the voltages and the dimensions are scaled down, while doping as well as current densities are increased by the scale factor α, keeping the vertical field constant. In addition to this, the speed of circuit is also enhanced by the same factor α and circuit density increases by α^2, however, the problem arises when the horizontal field keeps on increasing as the dimension of device becomes significantly smaller, creating problems on the potential barrier at the source end [25].

Also, the voltages, sub-threshold slope, and OFF-current are not scaled well as the length scales down, which violates the constant-field scaling technique [26]. Therefore, *Baccarani et. al.* [27] has proposed a more generalized scaling technique in which the vertical and horizontal fields are changed by the same multiplication factor. Although, the shape of the electric field is preserved now, it has potential issue such as significant enhancements in the power density. *Brews* [28, 29] also proposed a scaling method called sub-

threshold scaling which does not stress on a specific factor for scaling individual dimensions and allows independent manipulation of a large number of variables as long as the remaining variables compensate for these changes. The summary of these scaling is shown in Table 2.

However, the aforementioned scaling techniques only tell about how to shrink the device, it is unable to tell anything about the limit of the scaling. There are certain physical phenomena which limit these scaling techniques such as quantum mechanical tunneling that happens as the barrier existing in MOSFET becomes very thin and the random dopant fluctuation, due to the present manufacturing techniques.

Table 2. The scaling techniques [16].

Physical parameter	Constant Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric Field	1	ϵ	ϵ
Voltage	$1/\alpha$	ϵ/α	ϵ/α_d
On-current	$1/\alpha$	ϵ/α	ϵ/α_w
Doping	A	$\epsilon\alpha$	$\epsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w{}^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Power dissipation	$1/\alpha^2$	$\epsilon^{2/}\alpha^2$	$\epsilon^2/\alpha_w\alpha_d$

In addition to this, the power supply scaling also has a limit which is the thermal voltage [30]. The Si band-gap potential is the major parameter which cannot be scaled down, and as the supply voltage is scaled down, the effect of band-gap potential increases which results increase in the electric field and the depletion depth. Here, the band-gap potential can only be changed by changing the semiconductor itself. As the electric field increases, it confines more charge carrier closer to the surface, which further reduces the mobility, increases the quantum confinement energy and the gate depletion, and consequently increasing the threshold voltage.

Moreover, several methods are utilized to reduce the threshold voltage, i.e. retrograde doping profile and the body biasing relative to source etc. [31, 32]. Therefore, there is a need for proper selection of power supply voltage and threshold voltage [33]. Although it is widely believed that the CMOS will still be the dominant technology in near future, however the practical and fundamental limits of CMOS scaling poses tremendous challenges beyond the *45-nm* technology node. In addition to this, the major challenge faced by the circuit designers is the Short Channel Effects (SCE).

4. Short Channel Effects (SCEs)

When the MOSFET channel length (the distance between source and drain in the MOSFET) is comparable to the depletion depth of the source and drain beneath a gate with zero drain-source voltage, the device is considered to be short scaled. Table 3 summarizes the various short channel effects. As the dimension of device shrinks significantly, the short channel effects dominates over the device performance [34] and are attributed following two physical phenomenas:

a) The restriction imposed on electron drift characteristics in the channel, and

b) Alteration of the threshold voltage due to the short channel length.

Table 3. Various short channel effects.

Reference	Effect	Reason
[35-37]	Drain Induced Barrier Lowering (DIBL)	As the drain voltage increases, the potential barrier of the channel decreases and allows the flow of electrons between the source and drain even if the gate voltage is lower than that of the threshold voltage.
[38, 39]	Surface scattering	The electric field component in the direction of current flow increases due to the extension of the depletion layer in the channel. This further makes the surface mobility field dependent as the channel length becomes significantly smaller.
[40, 41]	Velocity saturation	For short channel devices, the current saturates because of the carrier velocity saturation in place of pinch-off point in the bulk MOSFET and current is independent of gate to source voltage. It happens when the dimensions of device are scaled down without lowering the voltages. Therefore the trans-conductance reduces in the saturation mode of operation.
[42, 43]	Hot electron effect	As the high energy electrons enter the oxide layer they are trapped, which rises the oxide charging that accumulates with time and degrades the device performance by increasing threshold voltage and affect adversely the gate's control on the drain current.
[27]	Threshold voltage roll-off	As the field pattern generated by the gate is 2-D for short channel devices because of closeness of source and drain, the threshold voltage varies with the channel length. The part of channel is already depleted, therefore significantly less voltage is required for the operation of MOSFET as the threshold voltage decreases.
[44]	Punch-through	Due to the proximity of drain and source, the depletion region of the drain and source extend into the channel and merge. Therefore, the current flow between the source and drain cannot be controlled by the applied gate bias.
[45, 46]	Oxide tunneling current	As the oxide thickness reduces the electric field increases, which further forces the current to flow in the gate terminal.
[47]	Reverse short	The retrograde doping profile results in point defects at the surface edge where the

	channel effect	impurity atoms pile up and increases the channel doping closer to the source/drain region. For the short channel devices the region with the enhanced doping is a significant part of the channel. Therefore, the increase in doping in addition to reduced channel length causes the threshold voltage to increase with scaling until eventually short channel effects take over.
[48, 49]	Gate Induced Drain Leakage (GIDL)	The electric field due to the drain can cause the overlap region to form a depletion region and if this field is significantly high it may invert the surface to p-type. When the channel is being formed the carriers are swept in this *p*-well. The effect of increase in the oxide thickness is more significant to GIDL as compared to that of the gate length.
[50, 51]	Mobility degradation	For the short channel devices, one reason for the decrease in mobility is the velocity saturation, which occurs due to the presence of electric field perpendicular to the gate. The electrons slow down by the increase in scattering, thereby decreasing the mobility with respect to the bulk MOSFET. Also, as the surface is rough, more scattering occurs.

However, the reduction of SCE is of prime concern while maintaining the better device performance in the nano-scale regime. Therefore, several methods have come up with some negative effects such as performance degradation and additional leakage. Due to increase in channel doping the electric field lines that originate from the drain and propagate to the source are terminated. This high level of doping degrades the low field mobility of the carrier as the impurity scattering is increased, which further reduces the drive current [52]. It also increases the Gate-Induced Drain Leakage (GIDL) and band-to-band tunneling across the reverse-biased drain junction. In addition to this, significantly threshold voltage variation has been observed due to statistical fluctuation of the channel dopants, mainly in the nano-scale regime [53]. The reduction of oxide thickness is important for improving the gate control on the channel, however, this causes tunnelling and results the leakage current when the thickness of the oxide reaches *2 nm* and further increases standby power [31, 54, 55]. However, with the lowering of source/drain junction depth to reduce drain coupling to the source barrier, the doping density has to be increased, however this doping density has an upper limit for solid solubility. Therefore, the series resistance increases and degrade the device performance [56, 57]. Table 4 suggests the certain scaling limits which introduce additional problems of SCEs.

Table 4. Limits of scaling [57].

Feature	Limit	Reason
Oxide thickness	*2.3 nm*	Leakage (I_{off})
Junction Depth	*30 nm*	Resistance (R_{sd})
Channel Doping	V_{th} = *0.25 V*	Leakage (I_{off})
Channel Length	*0.06 µm*	Leakage (I_{off})

With the scaling of MOSFET, the processing speed can be enhanced and further improved RF performance. The important metrics for RF MOSFET circuits are the maximum oscillation frequency and cut-off frequency. The former is defined as the frequency at which the current gain of the device becomes unity and later defines the frequency at which power gain becomes unity. However, both of these metrices relate to the trans-conductance and parasitic capacitance. As the dimension of device reduces, the cut-off frequency of device increases up to *400 GHz*. The noise-figure is also one of the other important figure-of-merit. *Cen and Song* [58] have purposed a new figure-of-merit for low noise amplifier and also predicted the close optimum gate voltage to maximize this figure-of-merit.

Fig. 6 shows the advances in MOSFET technologies which have continued with further increase in the cut-off frequency (f_T) of the devices [59]. Due to relatively high f_T values, the bulk-silicon MOSFET device is becoming a viable technology choice in the analog and RF applications for portable wireless communication systems.

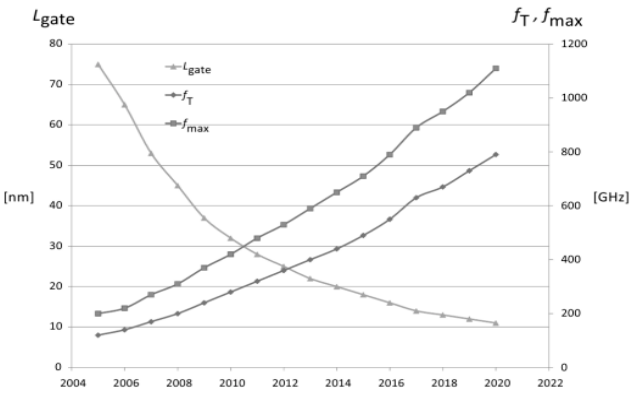


Fig. 6. Trend of MOSFET scaling [59].

It can also be seen through Fig. 7 that a high value of the current gain frequency can be achieved with the CMOS technology. However, with *18-nm* technology, the f_T of *511 GHz* is acheived, which shows that CMOS has an advantage for high speed applications in future communication system.

In addition to this, the low power dissipation of device is required for the applications such as battery operated single-chip wireless transceiver [60], which can be achieved by reducing the device supply voltage. Therefore, the communication market has reached a revolutionary era with the various forms of improvement in the MOSFET structure. The circuits formally implemented as a discrete structure, now, which is implemented on the single chip. Therefore, the system-on-chip is no longer a mere idea. Due to the high unity gain of MOSFET, it becomes an attraction for the RFIC circuit designers [61]. However, it has been observed that, the MOSFET must be operated in the moderately inverted region to achieve the desired circuit performance in ultra-low power RFIC design [62]. In addition to this, *Yin and Yuhua* [63] have analyzed the MOSFETs, which has higher low-frequency limit as compared with BJTs which is useful for RFIC design as well as generating High Frequency (HF) distortion model for MOSFETs and recently, new technologies acting as a driving force in the personal wireless communication area.

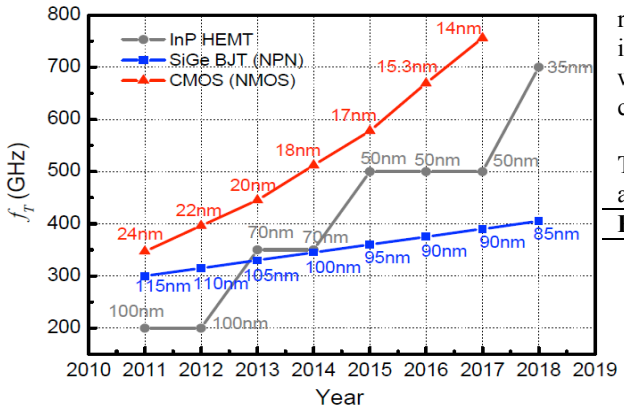


Fig. 7. The current-gain frequency variation over the years (ITRS 2011 update) [21].

Razavi [64] has presented the difficulty in using the digital MOS technology for the analog application. The trade-off is optimized, i.e. the power-speed trade-off, although a multidimensional design space in the form of octagon as in Fig. 8 is presented. Here every parameter is trade-off with each other. For example, to lower the noise of a front-end amplifier, we must consume a greater power or sacrifice linearity or to increase the gain of amplifier, we have to work on high supply voltage or sacrifice linearity. In addition to this, if the supply voltage is reduced, the power dissipation may increase. *Woerlee et. al.* [65] have confirmed the higher potential of CMOS for RF applications at *GHz* frequency.

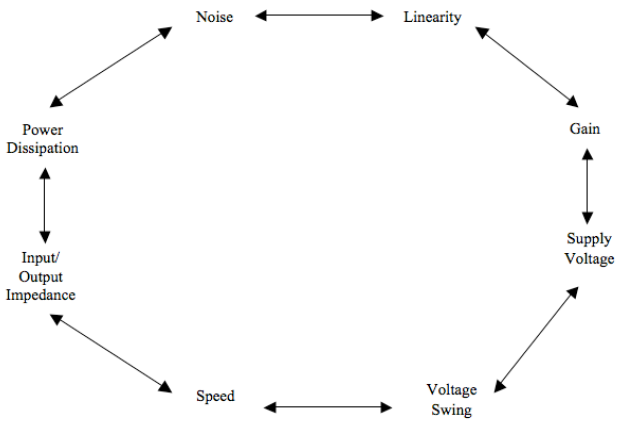


Fig. 8. The analog octagon [64].

Recently, various transceiver chips using the CMOS technology have been developed, as summarized in Table 5. The reduction of feature size of device based on the channel and gate engineering [35] also introduces additional parasitic and new phenomena such as SCE, parasitic source/drain resistance, poly-silicon depletion layer effect, ballistic transport, carrier energy quantization, bias dependent parasitic capacitances etc. As the fabrication processes also limits the scaling, novel techniques have to be introduced to keep the pace with the scaling to yield the desired throughput, and to retain the progress in device scaling technology.

To move forward in the direction to achieve better performance, a novel material and device structures, which are the non-conventional structures, are required beyond *65-nm* technology [72]. *Rue et. al.* [73] have analyzed that the output power capability of the transmitter will degrade as the device will scale down due to the hot-carrier injection and reducing the oxide will not be effective. Therefore, the innovated device structures can reduce the SCE and they would be a better choice to be used in the future transceiver chips, which are discussed in the following section.

Table 5. The recent single chip transceivers for different applications.

Reference	Technology	Application
[66]	*90-nm*	*5 Mbps* transceiver with energy harvesting module for wireless sensor network
[67]	*180-nm*	*2.4 GHz* low rate wireless personal area network (WPAN)
[68]	*90-nm*	*2.4 GHz* low power Zigbee transceiver
[69]	*28-nm*	Phase modulated continuous wave radar at *79 GHz*
[70]	*130-nm*	*24 GHz* UWB transceiver with self organizing localization network
[71]	*130-nm*	*3 GHz* to *10 GHz* front-end transceiver used for low power biomedical radar

5. Advanced MOSFET Structures

In the Silicon-On-Insulator (SOI) technology, the presence of buried oxide layer below the transistor junction reduces the junction capacitances and reverse body effect. It provides a faster and more power effective device. The SOI has been considered as one alternative to the conventional bulk MOSFET which offer performance as expected from the next generation Silicon technology [31]. By using the buried-oxide layer the fringing capacitances are suppressed, that provides better processing speed [74]. In the proposed CSDG MOSEFT, this fringing capacitance is not available (negligible) due to the circular Gate-All-Around (GAA) overlapping on the Drain (D) and Source (S). However, the fully-depleted MOSFET improves the SCE, transistor scalability, and circuit performance [75, 76]. The introduction of ultra-thin SOI technology offers the significant advantage of reduced leakage paths by stopping the penetration of drain electric field in the source region. However, this device suffers from degradation in the *ON-state* current due to mobility degradation and increases the external resistance, which can be rectified by the use of thin gate spacer with raised source/drain process. In addition to this, the threshold voltage control with the use of doping is difficult, therefore the poly-silicon gate is replaced with a metal silicide gate where it is controlled by the work function engineering by the gate. Moreover, the mobility degradation due to the surface roughness is still an issue when the body thickness reaches up to *5 nm* [77]. For the fully-depleted SOI MOSFETs, the drain electric field penetrates though the buried oxide into the channel region, thereby resulting in a large impact on the channel electrostatics. The bulk-MOSFETs and DG MOSFETs can achieve better short channel effect compared to that of the fully-depleted SOI MOSFETs due to the screening of channel by the bottom layer. Therefore, with the advantages of high processing speed, lower power dissipation and consumption, high tolerance to radiations, and low value of parasitic capacitances, some other unavoidable issues come

into picture when the SOI dimension reaches the nanometre scale regime [75].

To look at the possibilities for bulk-MOSFETs beyond the *45-nm* technology node, a number of novel multi-gate MOSFETs have been proposed, including Double-gate, Pi-gate [78], Omega-gate [79], Tri-gate [80], and Surrounding-gate MOSFETs. Various numerical simulations and analytical analysis have shown better scalability of multi-gate MOSFETs over the bulk MOSFETs. The improved scalability allows multi-gate MOSFETs to scale down to shorter gate length with the same *OFF-state* current or produce less *OFF-state* current with same gate length, thereby achieving better power-speed product. Among these new emerging devices, the DG MOSFET is the most promising because of its compatibility with the conventional planar technology. In addition to this, the DG MOSFET reduces the fringing field through drain-to-body which further improves the device scalability. The mobility requirement in this structure is less as compared to that of the bulk MOSFET due to less vertical field. However, the mobility can be enhanced by using the following techniques:

a) Strain engineering and

b) Orientation effects [81].

Therefore, more enhanced versions of SOI structures come into the practice, which is a thin body fully-depleted SOI MOSFET, raised source and drain fully-depleted SOI MOSFET, multiple-gate fully-depleted SOI MOSFET. Recently, to advance the scaling of MOSFET technology the double-gate MOSFET and surrounding-gate MOSFET using lightly doped and ultra-thin body layer are the emerging research area as discussed in ref. [82]. For the advancement in the technology for wireless communication areas, the standard MOSFET structures using the CMOS technology should be replaced by more innovative structures such as double-gate MOSFET and surrounding-gate MOSFET. The advantages of these structures for the operation in the high frequency regime of spectrum are discussed in the following sections.

6. Double-Gate (DG) MOSFET

The main design objectives of DG MOSFETs are to:

a) reduce SCE and

b) maintain good electrical characteristics [83].

The planer DG MOSFET is an extension of the single-gate MOSFET that consists of two gates designated as a front-gate and back-gate, within which the ultra thin silicon layer is sandwiched [84]. The additional gate significantly increases the electrostatic gate control over the channel and these gates are effective in shielding the drain electric field lines from approaching the source to reduce the potential barrier as well as reducing the SCE. Due to un-doped/lightly doped body, the problem of random dopant fluctuation is also removed. Moreover, both the gates contribute to inversion carriers, which have high drive capability and two channels for the current flow are formed, when these two gates simultaneously control the charge. In addition to this, as the Silicon film is very thin there exists a good coupling between the front and back gate, which affect the terminal characteristics of the MOSFET. Fig. 9 shows the schematic of DG MOSFET.

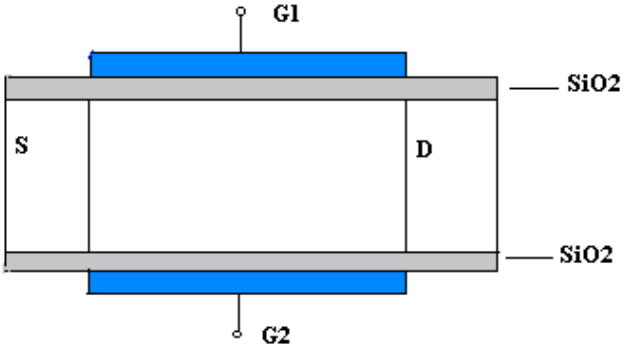


Fig. 9. Schematic of double-gate MOSFET.

In the common mode operation, both the gates are switched simultaneously, however for other possible mode of operation, back-gate bias is applied to create a conducting plane, and switch the front-gate which provides an additional parameter for the circuit design. Therefore, two types of structures are possible:

a) *Symmetric DG MOSFET:* both the gates have identical work function. However, the threshold voltage can be adjusted with the help of work function of gates. The thin silicon substrate is under volume inversion condition, therefore the conduction of carriers is across the entire volume of material as compared to that of the bulk devices.

b) *Asymmetric DG MOSFET:* both the gates have different work function. However, the threshold voltage can be adjusted by changing the body thickness and gate oxide thickness without need for special gate material. In the asymmetric double-gate device, two oxide thicknesses are unequal, the two gates have different flat-band voltage and two different gate biases. In the asymmetric DG MOSFET with a mid-gap gate electrode, the bands in silicon are not flat in the sub-threshold regime [85].

There are two operating modes for DG MOSFETs [86]:

a) *Three-terminal mode*: The three-terminal mode refers to the situation where the two gates of DG MOSFET are electrically connected and switched, simultaneously.

b) *Four-terminal driven (or independently driven) mode*: When operated in four-terminal driven mode, the two gates are biased differently with only one gate switching. The four-terminal driven mode enables the possibility of dynamic threshold voltage adjustment in circuit design and thus enlarges circuit design space.

Fig. 10 shows the different structures and two operating modes of the DG MOSFET. However, the four-terminal driven DG MOSFETs exhibits non-ideal sub-threshold slope. This is because the potential across the silicon film does not move along as a whole with the switching gate if the potential of the non-switching gate is fixed. The four-terminal driven DG MOSFET also shows worse short

channel effect than the commonly used three-terminal driven DG MOSFET.

Due to the high gate-to-substrate coupling, the device produces a near ideal sub-threshold slope (*60 mV/dec*) and flexible threshold voltage control can be offered by the separation of the two gates [87]. This device has less parasitic capacitances as compared to the conventional MOSFET, however the important thing is the proper alignment of the front and back gate, as the misalignment contributes to the parasitic capacitances. The body thickness has to be controlled to reduce the parasitic resistances, which are in series with the channel and source/drain electrode. When the scattering due to impurity or coulomb scattering is absent, then the carrier mobility is significantly high. The carrier mobility degradation which is related to gate field, reduces due to the lightly doped/undoped substrate film for the given oxide thickness. However, as both the gates are close to channel, there is the dominant control over the channel electrostatics.

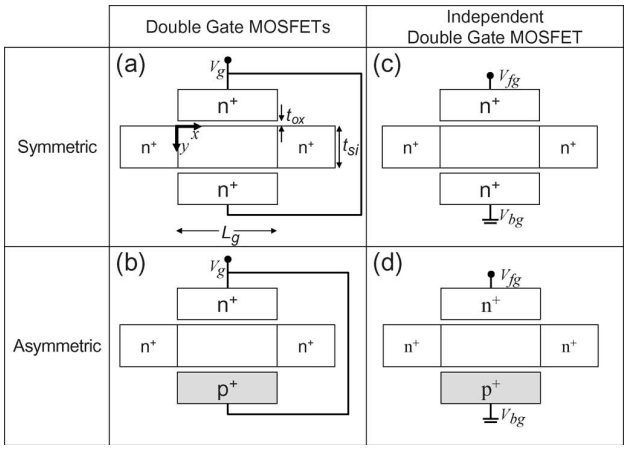


Fig. 10. Schematics of DG MOSFET structure for tied gates and separated gates [86].

The double-gate MOSFET has an advantage of the architectural feature which is useful for the design of extraordinarily radio-frequency analog integrated circuits and adaptive systems, with less difficulty in fabrication processes. Although, it is pointed out that the device has much better potential in this form of application, if the top and bottom gates are driven independently [88]. This increases the operational capability, reduces the parasitic capacitances and layout area, and increasing the speed with reduced the power consumption as compared to that of the conventional MOSFET's. Moreover, this is a useful method to tune the response of conventional CMOS analog circuits, especially, for the current mode design [89]. The DG MOSFETs cover the way for capable, tolerant and reduced circuit size with tuneable features.

Various researchers/scientists have devoted their work in developing compact models for DG MOSFET. *Balestra et. al.* [90] demonstrated that the double-gate MOSFET force the whole silicon body thickness in the strong inversion. The volume-inversion effect is quite significant when the gate-source voltage is less than the threshold voltage. With the increase in gate voltage, the potential increases at the surface as the channel is formed on the surface and minimum electric potential lies at center of the body $x = 0$, due to the screening of center of the silicon body by the charges on the surface as shown in Fig. 11(a). In addition to this, the significant effect can be seen when the $V_{gs} = 0.412\ V$ and $V_{gs} = 0.845\ V$. Fig. 11(b) also illustrates the similar volume-inversion concept. The volume inversion effect is significantly up to the threshold voltage, $V_{th} = 0.4\ V$ but as the gate voltage crosses the threshold voltage, the surface and center potentials are decoupled.

The center potential saturates at a specific potential value as the arcsine argument cannot exceed beyond $\pi/2$ but the surface potential keeps on increasing. It is illustrated through the Fig. 11(b) that the surface potential variation above the threshold voltage is independent of the silicon body thickness. In addition to this, *Taur et. al.* [91] have also presented an analytical model based on the charge sheet approximation for symmetric double-gate MOSFET and analyzed the threshold voltage (V_{th}), which is independent of the silicon body thickness (t_{si}). However, an exponential decrease in the saturated value of current with the drain to source voltage (V_{ds}) is observed, as compared to the common piecewise models where the current is made to be constant in saturation. The potential distribution of asymmetric DG MOSFET is linear due to the presence of initial electric field as shown in Fig. 12. However, the minimum potential lies outside the range of Silicon body thickness. As the gate voltage increases this electric field reduces, therefore for $V_{gs} = 1.40\ V$ the potential variation is approximated as parabolic where the minimum potential approaches to the center of Silicon film. *Lu and Taur* [92] have purposed a model based on the *Poisson equation* and the current continuity equation, without the charge sheet approximation. Moreover, the authors presented the threshold voltage of asymetric DG MOSFETs that is the function of Silicon thickness. Therefore, the sub-threshold current is much more sensitive to the Silicon film thickness, as compared to that of the symmetric DG MOSFET. However, the ADG MOSFET with thicker Silicon film has a lower threshold voltage and thus higher sub-threshold current. In addition to this, as illustrated in Fig. 13, the reduction in threshold voltage with the reduction in the oxide thickness results in higher subthreshold current. *Conde et. al.* [93] have developed an accurate drain current model consistent with the drift-diffusion transport and based on the *Pierret and Shields formulation* which is valid for all the operating conditions. In addition to this, *Conde et. al.* [94] also developed the analytical solution for the surface potential of undoped body symmetric DG MOSFET using the principle branch of the *Lambert W function*.

However, for achieving the desired circuit performance of DG structure, *Balasubramaniam et. al.* [95] have analyzed the effective channel length that is larger than that of the physical gate length, and the circuit performance is enhanced by using the thin body DG MOSFET. The effect of random dopant fluctuation and junction capacitances is reduced significantly as the lightly doped or undoped body is used, respectively. The variation in the source drain separation for achieving a better drive current can be performed, however the trade-off between SCE with series resistance has to be maintained. The result illustrated that the optimal gate to source-drain overlap for maximizing the circuit performance is less than the needed to maximize the drive current [95]. *Cross et. al.* [96] investigated the *non-Colombian scattering* and the reason behind the degradation of mobility below *100 nm* gate, arising because of the presence of neutral defects in *Si* or at the interface near the source and drain. The authors also illustrated that the defects can be improved by annealing temperature from $1050\ ^oC$ to $1080\ ^oC$.

Srivastava et. al. [97] investigated the effect of the gate and channel engineering on the device which would further

improved the circuit speed and power consumption. The author's results demonstrate that the DG MOSFET has better performance as compared to that of the other counterparts. The Fringing Induced Barrier Lower (FIBL) studied by *Charmi et. al.* [98] have been arises when the effective oxide thickness is comparable to that of the gate length. Moreover, the reduction of FIBL can be performed by using under-lap source/drain region. *Evans et. al.* [99] have analyzed that the carrier penetration into the oxide is not accounted for in the density gradient method, therefore the first principle computation can be used to optimize an accuracy of the density gradient method for modeling of the device. The position of the impurity in the channel plays a significant role and it degrades the current in the device. Therefore *Dollfus et. al.* [100] have analyzed this effect on the single-gate MOSFET as well as DG MOSFET in addition to the velocity overshoot effect for both the device structures. *Dollfus et. al.* [100] have illustrated that the degradation in the performance of single-gate MOSFET is more pronounced with significant effect observed for the *p*-type impurity.

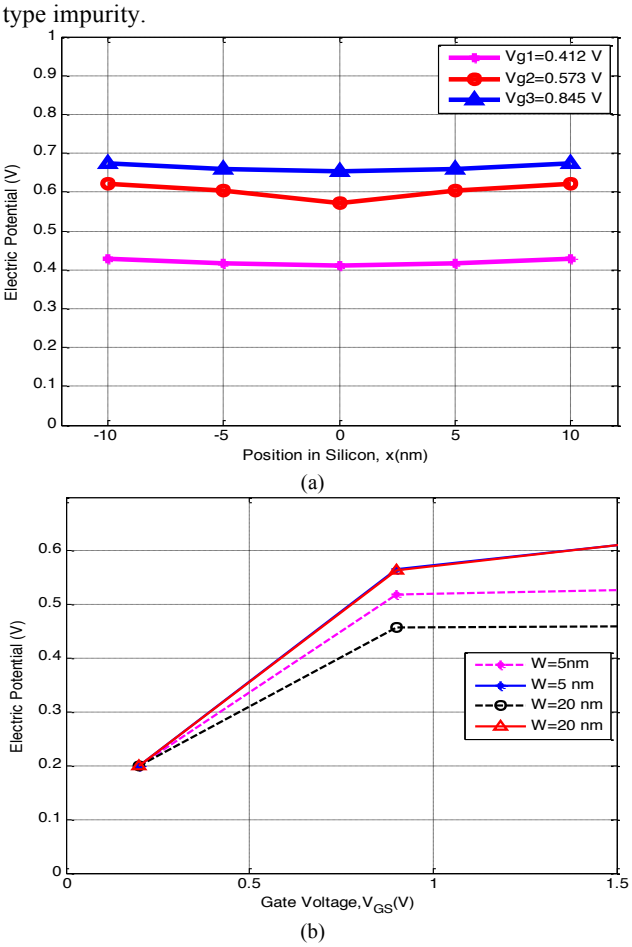


Fig. 11. Symmetric DG MOSFET electric potential distribtion at (a) various positions in the Si-body thickness and (b) different gate-source voltages.

For a DG MOSFET, the effect of negative gate overlap and the control of back gate bias has been analyzed by *Shao and Yu* [101], which illustrate that if the overlap is negative, the device performance is degraded. However, if the back gate bias is high, the threshold voltage is reduced which further increases the circuit speed due to the increase in the ion and if the bias is low, the threshold voltage is increased, which can reduce the power dissipation. Therefore, depending on the application, a trade-off can be maintained in high *ON-state* current and low power dissipation. Based on the charge coupling between the source and drain end and the front and back surface potential, *Conde et. al.* [102] have developed the drain current and the trans-conductance model for the undoped asymmetric DG MOSFET.

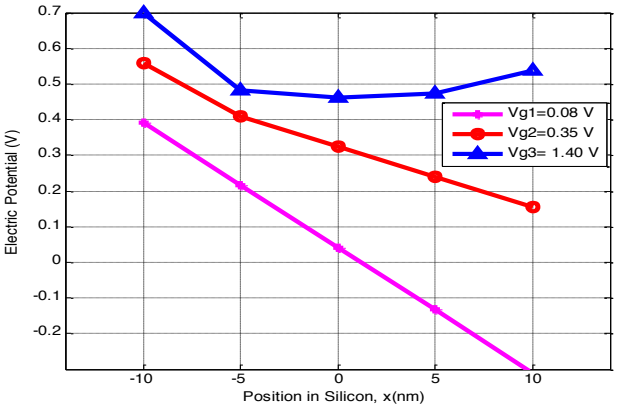


Fig. 12. Asymmetric DG MOSFET electric potential distribution at various positions in Si-body thickness.

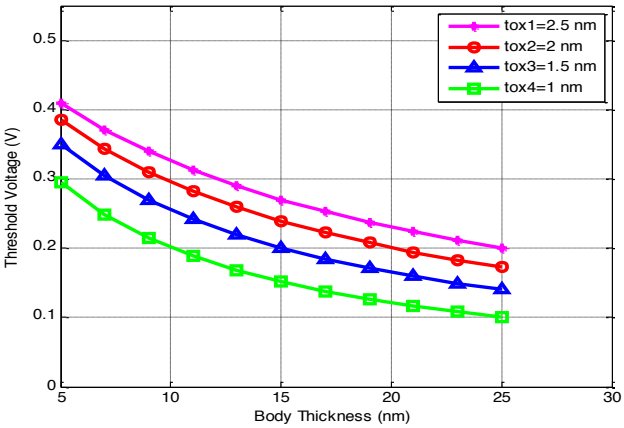


Fig. 13. Threshold voltage of asymmetric DG MOSFET.

The variation of trans-conductance and sub-threshold slope has been analyzed based on the variation of back gate bias. *Taur* [103] has analyzed a undoped body asymmetric DG MOSFET, the symmetry point shifts from the center to some point in the Silicon body and is minimum at that point. Moreover, the threshold voltage dependencies on the dimensions of asymmetric DG MOSFET have been studied for the long and short channel and then compared with the threshold variation with a symmetric DG MOSFET in ref. [104]. *Cakici and Roy* [105] have performed a case study on *Schmitt trigger* to analyze the effect of using connected gates or independent gates DG MOSFET and the results illustrate that the high noise immunity at low dynamic power dissipation can be achieved by the independent operating gates. Although, an increase in the delay, leakage power and process variation are the significant undesirable bi-products for the device performance. The dynamic threshold voltage control is feasible with the use of independent gates DG technology. In addition to this, *Srivastava et. al.* [106] have explored the design possibilities of the double gate MOSFET for achieving low power application. *Roy et. al.* [107] have developed a model for a low density of state material in DG MOSFET by using both *Fermi-Dirac statistics* and *field dependent diffusivity*. A compact model has been developed in ref. [108] for a junctionless DG MOSFET. *Mattausch et. al.* [109] pointed out that to the future requirements of the technology, the surface potential model based on drift-diffusion approximation is essential.

However, *Wie et. al.* [110] have presented that the minimum channel length of the DG SOI MOSFET can be reduced to *30 %* as compared to that of the conventional MOSFET, which would further increase the cut-off frequency and making it a better candidate for low voltage and low power applications. *Mohankumar et. al.* [111] have explored the influence of channel and gate engineering on the analog/RF performance of DG MOSFET. The channel engineered devices show the reduction of the cut-off frequency. The advantages of triple material DG MOSFET over the dual material and single material DG MOSFET has been discussed in ref. [112]. The authors have analyzed the performance enhancement in terms of the intrinsic gain of *20.41 %* and *38.53 %* for dual material DG MOSFET and triple material DG MOSFET, respectively. Further, the unity gain frequency of *14.23%* and *26.4%* for dual material DG MOSFET and triple material DG MOSFET, respectively, and the maximum oscillation frequency of *13.9 %* and *23.85 %* for dual material DG MOSFET and the triple material DG MOSFET, respectively. This shows that the device structure can provide enhanced performance for high frequency RF applications. *Mohankumar et. al.* [113] have analyzed the SCE reduction and RF performance enhancement of the single halo dual material DG MOSFET compared to the single halo counterpart. The realization of high performance analog and RF circuits are possible by the use of high dielectric DG MOSFET [114].

7. Surrounding-Gate MOSFET

The structure of surrounding-gate MOSFET (also known as cylindrical surrounding MOSFET) is rotated structure of single-gate MOSFET. In this structure, the channel is surrounded by the gate from all sides which reduces the leakage current in the device and further the performance of the device increases. Moreover, it also provides reduction in the length of device is achieved compared to DG MOSFET with a given silicon body thickness (t_{si}) and oxide thickness (t_{ox}) which further increases the packing density [115]. The current flow is vertical along the cylindrical Si/SiO_2 interface and the gate length of transistor is defined by the height of the gate material. The tight capacitive coupling in all direction reduces the SCE. The general surrounding-gate MOSFET structure is shown in Fig. 14. However, the vertical orientation of the device on a single-chip reduces the chip area and is also a potential research area.

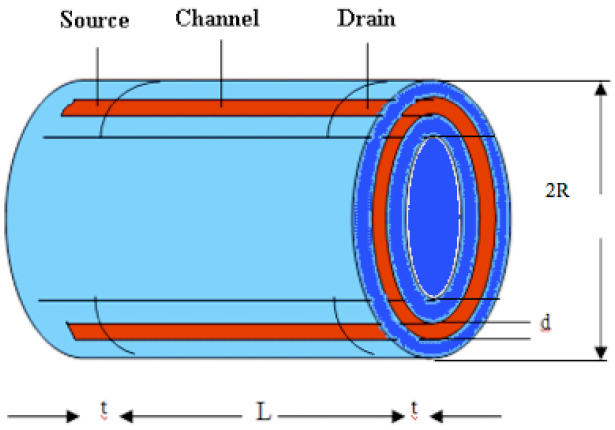
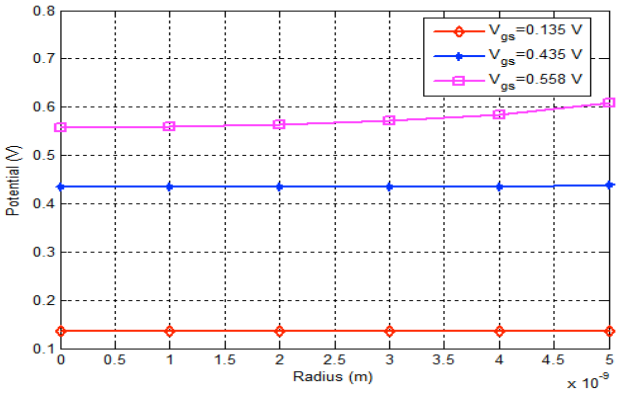
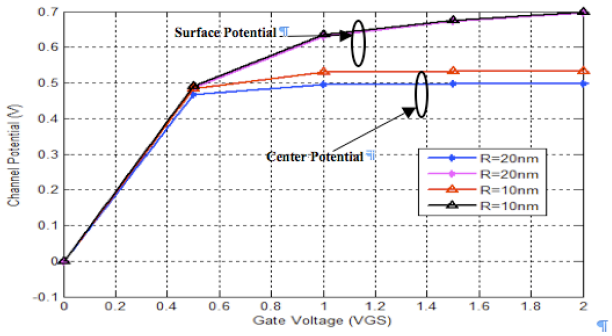


Fig. 14. Schematic of surrounding-gate MOSFET.

The surrounding-gate MOSFET is very effectively scaled down to the nanometer regime for low power and high speed applications [116]. *Rustagi et. al.* [117] have analyzed the surrounding-gate MOSFET, which is very effective for the high speed and low power circuit applications. *Iniguez et. al.* [118] have developed a DC model for surrounding-gate MOSFET based on the charge controlled model, and the continuity of the channel current, which is preserved throughout all the operating regions therefore the model is effective for circuit simulations. *Jimenez et. al.* [119] have also developed a model for the lightly doped surrounding-gate MOSFET without any fitting parameter. *Bian et. al.* [120] have derived a model based on both the drift and diffusion current components with the analytical potential approach, including the potentials at the oxide silicon interface and silicon center as illustrated in Fig. 15. However, the model in not applicable for the accumulation region. The authors have formulated the drain current based on the *Pao-Sah integral*. The validity of model is analyzed with different radius and oxide thicknesses. Fig. 15(a) represents that when the gate-source voltage is less than that of the threshold voltage, the volume inversion effect is quite significant (V_{gs} = *0.135 V* and V_{gs} = *0.435 V*) and the potential is constant across the radius of the cylinder, but at the gate-source voltage exceeds the threshold voltage (V_{gs} = *0.558 V*), the potential at the surface side increases as compared to the centre potential due to the formation of a channel on the surface of device.



(a)



(b)

Fig. 15. Symmetric DG MOSFET electric potential distribution at various (a) positions in the Si-body thickness, and (b) gate to source voltage, for various radius of cylinder (R).

Fig. 15(b) represents the variation of center and surface potential with the gate-to-source voltage for different values of radius of cylinder R. The variation in R affects the center potential significantly compared to that of the surface potential, as the central portion of the device is at the longer distance from the gate, therefore for the higher value of R, the central potential is significantly low. *Yu* [121] has

developed a model for the depletion mode surrounding gate nano-wire FET with capturing the conduction mechanism from sub-threshold to saturation region. The model for surrounding-gate MOSFET has been developed by taking into account the polysilicon depletion effect [122]. However, *Roy et. al.* [123] have developed a model for the surrounding-gate MOSFET based on *Gaussian law* instead of *Poisson equation*.

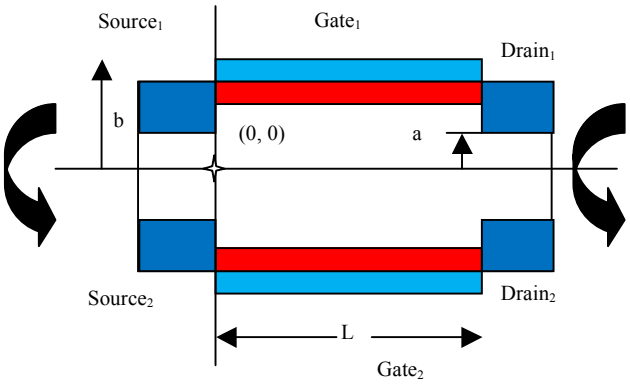
A potential based model for the dual material surrounding-gate MOSFET before the onset of strong inversion has been analyzed in ref. [125] based on parabolic approximation to understand the short channel effects due to gate engineering. A new technique of general series solution method is also developed for solving the *Cylindrical Poisson equation* which is very effective in observing the various short channel effects that is threshold voltage, Drain Induced Barrier Lowering (DIBL) etc. [126]. The high level of doping and ultra thin oxide is a major requirement to reduce these short channel effects. *Pandian and Balamurugun* [127] have proposed a threshold voltage based model for the short channel surrounding-gate nano-wire transistors with two forms of geometry that is junction based surrounding-gate MOSFET and rectangular surrounding-gate MOSFET. The major difference between these two geometries are: the rectangular-gate device is bound to get affected by corner effects much more in comparison with the cylindrical-gate device. A model for surrounding-gate MOSFET including different fringing gate capacitance was developed, which is valid for the short channel devices with $L_g = 15\ nm$ and long channel devices with $L_g = 50\ nm$ [128]. However, based on the charge control model, the authors in ref. [129] developed an analytical expression of the total capacitance of undoped body surrounding-gate MOSFET as a function of voltages.

Kranti et. al. [130] have developed a model for the short channel surrounding-gate MOSFET accounting for the effect of field dependent mobility, velocity saturation, and source-drain resistance effect. *Ruiz et. al.* [131] have developed a model for the total gate capacitance of surrounding-gate transistors and based on the result the authors have compared the capacitance behaviour of the DG MOSFET and surrounding-gate MOSFET and illustrated that the capacitance is less in surrounding-gate MOSFET as compared to DG MOSFET due to the greater confinement by the gate.

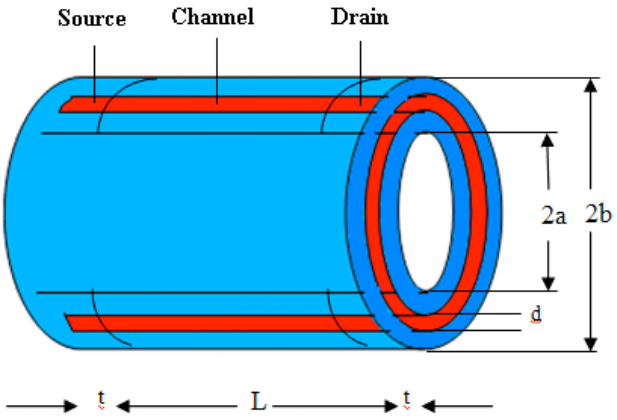
A comparative study of the single material gate and gate material engineering surrounding-gate MOSFET has been performed in ref. [132]. In addition to this, the effect of interface trap charges on the RF and linear distortion analysis also has been presented. The results indicate that the gate material engineered surrounding-gate MOSFET provides a better immunity against the interface charges and can maintain efficient device linearization, which makes the device useful for the radio frequency integrated circuit application. Moreover, the gate material engineered transistor shows better immunity against the influence of interface trap charges and exhibits significant enhancement to maintain the device linearization, as compared to a single material gate junction-less surrounding-gate MOSFET, so that it can be used as a high-efficiency linear radio-frequency integrated-circuit design and wireless applications. Cylindrical-gate MOSFET with the vacuum as the dielectric can be a better candidate for the high speed and high frequency applications with the reduced device size (compared to the other dielectric materials). The authors [133] have proposed an intrinsic small-signal equivalent circuit model of cylindrical / surrounded-gate MOSFET by which scattering parameters (S_{11}, S_{12}, S_{21}, and S_{22}) can be obtained. Although, the trans-conductance and *ON-state* drain current is reduced, but it can be enhanced by using the modification in gate and channel.

8. Cylindrical Surrounding Double-Gate (CSDG) MOSFET

With the development of surrounding-gate MOSFET in the nano-meter scale regime, the high frequency capability of the transistors has reached to the *GHz* and *THz* regime which is well suited for the radio frequency circuit applications [134, 135]. The structure of CSDG MOSFET is rotated structure of DG MOSFET. In this structure, the channel is surrounded by the gate from two sides (external and internal) which efficiently reduces the leakage current in the device and further the performance of the device increases. *Srivastava et. al.* [136, 137] have discussed the full gate control over the channel and proposed a model, named as CSDG)MOSFET in *2011* is shown in Fig. 16. This structure is based on the hollow Silicon cylinder and the gates are designed on the both side of the channel as external gate and internal gate. This device can achieve low *OFF-state* current, which makes the CSDG MOSFET as a promising device for Very Large Scale Integration (VLSI) and Ultra Large Scale Integration (ULSI) technology.



(a)



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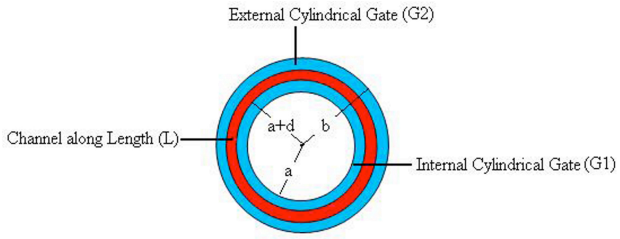

(c)

Fig. 16. Schematic of (a) DG MOSFET, (b) three dimensional CSDG MOSFET, and (c) side view of CSDG MOSFET [136].

After designing of this CSDG MOSFET, the authors [136, 137] have drawn the layout and simulate the parameters available in this design. It includes the basics of the circuit elements parameter required for the radio frequency sub-systems of the integrated circuits such as drain current, output voltage, threshold voltage, capacitances, resistances at switch *ON*-state, oxide thickness, resistance of poly-silicon, energy stored, cross talk, number of bulk capacitors, and power or voltage gain with the help of Fig. 17.

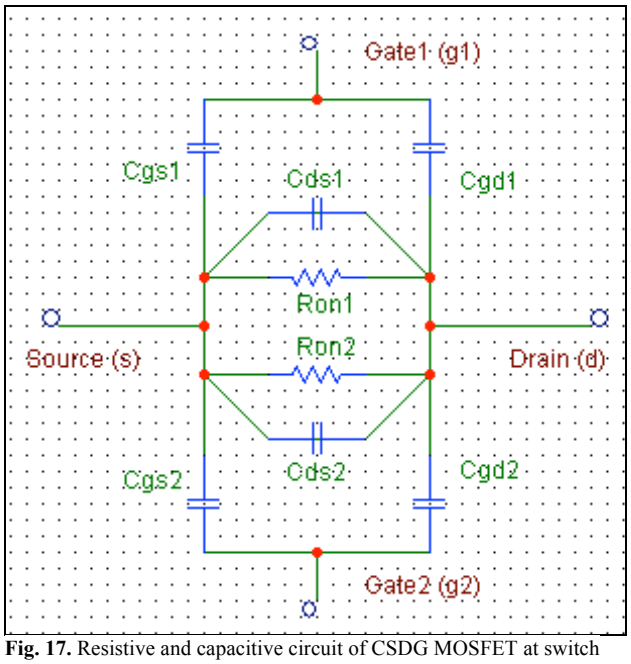

Fig. 17. Resistive and capacitive circuit of CSDG MOSFET at switch ON-state [136].

The model becomes explicit by using appropriate expressions for the channel charge densities in terms of applied voltages. The channel charge distribution in Si-film is adequately accounted for the charge control model. The physics based model of CSDG nano-wire MOSFET has been presented in ref. [138]. In this work, the authors presented a threshold voltage modelling using extrapolation method in strong inversion region. They obtained that CSDG MOSFET performs better than cylindrical surrounding-gate MOSFET. The TCAD analysis of CSDG MOSFET has been presented in ref. [139] which has incorporated an inner charge control gate. The CSDG MOSFET imerged as an improved electrostatic integrity with better RF performance. A remarkable cut off frequency of more than *2.3 THz* has been achieved. The drain current and noise model of CSDG MOSFET for RF switch has been analyses in ref. [140]. *Srivastava and Singh* [141] have performed a testing of CSDG MOSFET parameters using image acquisition and emphasized on the basics of the single image sensor for two dimensional images of a three dimension devices. It is usful for obtaining a satisfactory device parameter. This CSDG MOSFET has various perspective applications such as bridge rectifier [142], amplifier [143], Filters [144], satellite communications [145], etc.

9. Conclusions and Future Aspects

The demand of communication industry is increasing for the developments of devices to handle high data rate and high frequency operation. Moreover, the improvement in the communication market is also critically dependent on the dimension reduction of the devices. However, the conventional scaling, a tool for MOS technology advancement into the nano-scale regime has been hindered by various factors like the SCE, channel carrier mobility degradation, process variations etc. These are vital concern for the circuit designers, which further results in the significant control of drain on the channel potential. Therefore, the possible need is to minimize the effects of the drain on the channel potential that inspire numerous researchers/scientists for other non-conventional structures like SOI, pie-gate, and omega-gate MOSFET.

In this review, a lot of importance is being given on the DG MOSFET, surrounding-gate MOSFET and CSDG MOSFET, as these devices scale down to the shortest channel length possible for a chosen oxide thickness, which further reduces the short channel effects. Therefore, this analysis focuses on the review of DG MOSFET, surrounding-gate MOSFET and CSDG MOSFET modelling and device characterization for the high frequency applications. This article also discusses about the feasibility and the future challenges of device for use in the integrated circuits/system on chip. This would prove high packaging density and increase of performance in terms of unity-gain frequency and maximum oscillation frequency, in high frequency regime of the spectrum that is the *THz*, where the data rate approaches *100 Gbit/sec*. However, the gate and channel engineering would also be providing wide range of advantages for the application in high frequency applications. The communication in THz range remains a wide research area for the RF circuit designers and the communication industry.

Beyond the analyzed parameters, the CSDG MOSFET has potential challenges such as fabrication of this kind of devices by a tricky process, which can be reported in the future communications. Moreover, the dual material gate gradual channel cylindrical MOSFET has the highest cut-off frequency. The dual material gate junction-less transistor has an advantage of high *ON-state* drain current, high unity gain frequency, and high maximum oscillation frequency. These parameters can be carryover in the future research. The analysis of the various applications of CSDG MOSFET has good scope in near future.

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