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Design of a Low-power CMOS Level Shifter for Low-delay SoCs in Silterra 0.13 µm CMOS Process

Mohammad Torikul Islam Badal, Mamun Bin Ibne Reaz, Araf Farayez, Siti A. B. Ramli, Noorfazila Kamal

Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi, 43600, Selangor, Malaysia

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Abstract

Level Shifter (LS) circuits are widely used as interfaces for multiple voltage domains in moderns ICs and System on Chips (SoCs). Low power dissipation and low delay are the main design considerations for high performance level shifters. This paper presents the design of a level shifter integrating new topological modifications to assure a wide range of voltage conversion with low power dissipation and low output delay. The presented level shifter is designed to take input signal of 1 V and convert that into an output signal of 1.8 V which is simulated in Silterra 0.13 µm CMOS process. The post layout simulation results show that the designed LS circuit has a significant low power dissipation of only 0.1449 nW and low output delay of 25.55 ps covering only 17.36× 14.560 µm2 chip area. Through detailed comparison with recently reported LS circuits, it has been shown that the proposed level shifter achieved a better performance in terms of power consumption, delay and compact chip size.

Keywords: CMOS, Delay, Level Shifter, Multi-supply voltage design, SoC, Ultra-Low Power

1. Introduction

In the era of Complementary metal-oxide-semiconductor (CMOS) technology, low power consumption is one of the most key concerns to address in today's SoCs designs. The demand for low power and low output delay is very high, especially for handheld devices like cell phone, tablet etc. [1]. CMOS technology is being widely used to meet the increasing demand for low power consumption and low delay operation in microelectronics circuit systems [2] [3]. Considerable reduction in chip size (<1 mm^2) has become possible with the advancement of CMOS technology which minimizes the manufacturing cost greatly. In multi-voltage systems, level shifter is a significant circuit component and usually used in between core circuit and input/output (I/O) circuit [4]. Level Shifters are used to convert the voltage level of an input signal to another voltage level at the output node. But the conventional level shifter dissipates high power and suffers from longer delay variation. Hence, the low power dissipation and low operation delay in level shifter have become major design issues for microelectronics circuits. Increases in power dissipation cause rise in reliability issues and limit the device portability [5] [6]. To meet the increasing demand for low power and high performance ICs, CMOS technology is being aggressively scaled [7]. The most effective way to minimize power dissipation in VLSI and other electronic circuit is to minimize their corresponding supply voltages. This is because of the quadratic dependence of the power dissipation on the supply voltage [2]. The delay variation occurs due to different current driving capabilities of transistors [8] [9]. The level shifters are required to function appropriately when the difference between the two voltage levels is high. The high voltage difference may cause the failure of functionality in conventional LS circuit topologies due to low drive current when the supply voltage is very low [10] [11]. For the purpose of getting lower voltage from the high voltage domain, implementing CMOS inverters are normally adequate [12-14]]. But to get higher voltage from a low voltage supply domain in LS circuits, complicated circuit architectures are required. In order to design a simple LS circuit, proper design techniques must be utilized to balance the units of the circuit functioning at the high power supply voltage (VDDH) level with the input unit driving capability of the Level shifter [9] [15].

The differential cascade voltage switch (DCVS) topology described in figure 1 is considered as the traditional topology for LS circuit design. It comprises a half-latch composed of a pair of NMOS devices monitored by the differential low-voltage input signals A and AN and two PMOS transistors (MP2 and MP3). The topology acts as a ratioed circuit and there is a controversy between MN2 (MN3) and MP2 (MP3). As a result, to assure the accurate functionality proper balance must be maintained between the pull-down and pull-up strengths. In the CMOS circuit design, this requirement is very challenging to achieve when the input signals work around the threshold voltage levels [12]

To face the current rising issues of LS design, different methods have been proposed by different researchers in the last few years. Zhai et al. have proposed an architecture based on four DCVS cascaded circuits which convert 200 mV to 1.2 V [4]. This architecture upgrades the voltage

*E-mail address: torikul@siswa.ukm.edu.my
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gradually having an interval of 0.01 V in each conversion stage and every conversion stage utilizes its respective VDDH. But this architecture required multiple numbers of power regulators to produce intermediate VDDHs which causes high power consumption. The LS solution suggested by Chen et al. [12] employed two PMOS current limiters in the conventional DCVS configuration. It minimizes the drive strength of the half-latch pull-up network. This design needs a reference path which should be kept "on" all the time for the current limiters to convert the sub-threshold input signals. It is considered as the main disadvantage of this architecture which is also responsible for greater static power dissipation. The Wooterset al. reported LS topology a single supply level shifter for low power and high speed applications composed of two stages [8]. The first stage is the conventional DCVS circuit which is used to generate rail to rail swing. The second stage is the combination of the DCVS circuit and all time "on" diode connected NMOS transistor at the top. Although the design has the capability of transforming low voltage signals to high voltage signals, the power dissipation and output delay of the designed circuit still remain high. This approach escapes intermediate power lines, but is unable to achieve high-speed performance. The drive strength of the pull-up network is controlled by off-biased and diode-connected PMOS transistors in [17]. Additionally, to tradeoff power consumption and speed, multi-threshold CMOS design strategy is integrated into this design. It is difficult to achieve all-time off-biased PMOS transistors, especially in terms of both dynamic energy consumption and static power. Moreover, it has a negative impact on overall power consumption. To address the design issue, few other designs are presented in the literature [18-22]. Among these solutions, level shifter circuits designed in [18, 19, 21] depend on the difference of voltage supply.

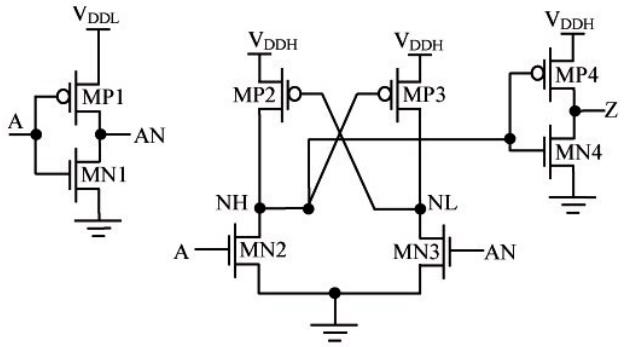

Fig. 1. Conventional DCVS level converter [16]

The LS requires a fast delay to achieve a high performance. Even though various types of CMOS LS architecture are available, designers tend to use the simplest and easily integrable LS schemes. Therefore, the main challenge faced by the designers is to design a high-performance LS with simple LS architecture. To meet the demand of low power dissipation and low operation delay attributes, an improved LS design implemented in Silterra 0.13um CMOS process is presented in this article. The main challenge of designing an effective various-supply circuit is minimizing the cost of the level conversion between several voltage domains and at the same time keeping the total robustness of the design.

2. Methodology

The schematic of a conventional basic Level shifter is presented in figure 1. The circuit is operated by equivalent input signals IN and INB. It is composed of cross-coupled two NMOS driver transistors (MN_1, MN_2) and PMOS latch (MP_1, MP_2). The functionality of the circuit fails when there is a large difference between the high supply voltage V_{DDH} and low supply voltage V_{DDL}. When the voltage IN and INB are low, the MN1 and MN2 go off and MN1 and MN2 turn on when the IN and INB are high, respectively. MP_1 will turn ON when the MN_2 pulls down the node OUT. Then MP_2 goes OFF and OUT will drop down to the GROUND level because the node OUTB increases to VDDH. Furthermore, the voltage of OUT is derived by both pull-down transistor MN_2 and drive current of pull-up transistors MP_2. Therefore, OUT can't be discharged if the drive current of MP_2 is higher compared to MN_2. On the other hand, the OUT can't be discharged when IN is high and INB is low, and the transistors MN_1 and MN_2 are turned ON and OFF respectively. Thus, the conventional LS circuit cannot function properly in this state.

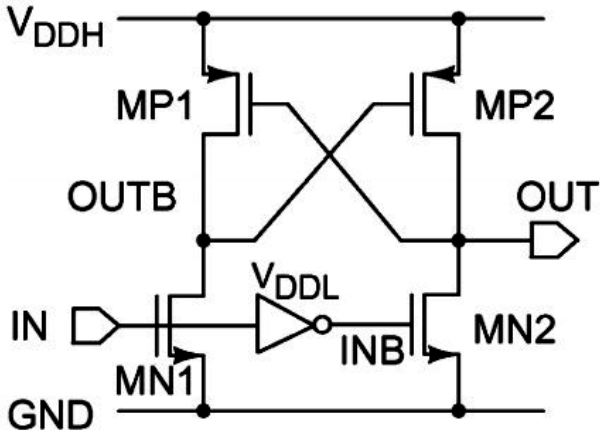

Fig. 2. Schematic of the basic level shifter [1]

The Schematic of the proposed level shifter circuit is presented in Figure 3. In this circuit, when the input is at 0 V, M_6 and M_8 turn on and off respectively while node N_2 discharges through M_3. Node N_3 charges to VDD forcing the M_5 to go to off state and thus the output discharges to 0 V. M_8 turns on and node N_2 initially discharges through M_3 when the input transition is high. The M_5 turns on when the node N_3 is discharged. When the node N_2 is charged up to VDD, the M_6 turns off. In the designed level shifter circuit, the main focus was to reduce the power dissipation and the output delay by modifying the dimensions of the transistors. The dynamic power dissipation can be decreased by minimizing the size of the gate which in turn reduces both the width and the length of the transistor [16]. Different dimensions of the transistors width and length (W/L) were used to design the proposed circuit as described in table 1. Each design condition specifies a unique pair of width by length ratios for NMOS and PMOS. Multiple numbers of design conditions had been carried out to find the best W/L ratios to achieve design goals.

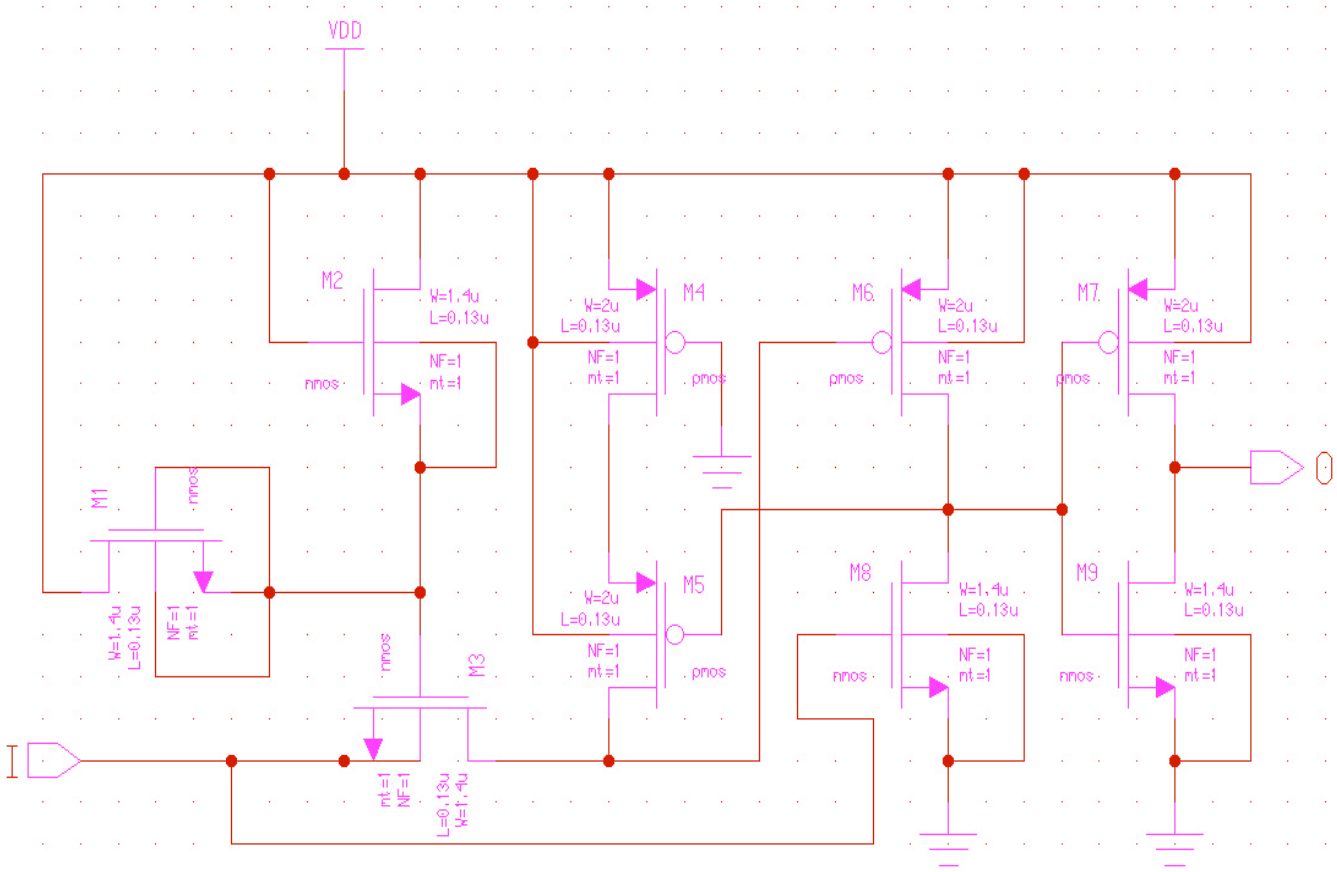

Fig. 3. Schematic of the proposed level shifter circuit

Table 1. Transistor sizes of the proposed level shifter circuit

Transistors	Design 1 (W/L)	Design 2 (W/L)	Design 3 (W/L)	Design 4 (W/L)	Design 5 (W/L)
PMOS	2.0µ /0.13µ	2.0µ /0.13µ	1.4µ /0.13µ	1.4µ /0.13µ	1.0µ /0.13µ
NMOS	2.0µ /0.13µ	1.4µ /0.13µ	1.4µ /0.13µ	1.0µ /0.13µ	1.0µ /0.13µ

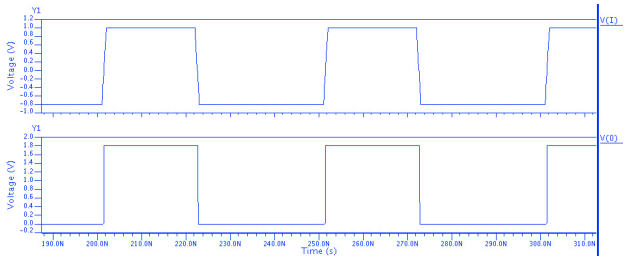

Fig. 4. The voltage conversion of the proposed level shifter of design 1

3. Results and Discussion

The proposed level shifter is designed and simulated in Silterra 0.13µm CMOS process. The channel length of all PMOS and NMOS are taken as 0.13µm. The given input voltage for all the five designs is 1V and the achieved high output voltage is 1.8 V. Figures 4, 6, 8, 10 and 12 illustrate the input and output waveforms for each of the five designs. It can be observed from the respective figures that the output waveforms have similar wave shapes to their corresponding input signals, but there is a change in the peak of all the output waveforms. The proposed level shifters were able to perform voltage level shifting from low to high voltage level. Figures 5, 7, 9, 11 and 13 illustrate more zoomed versions of the input and output voltage waveforms to illustrate the measurement of the output delay.

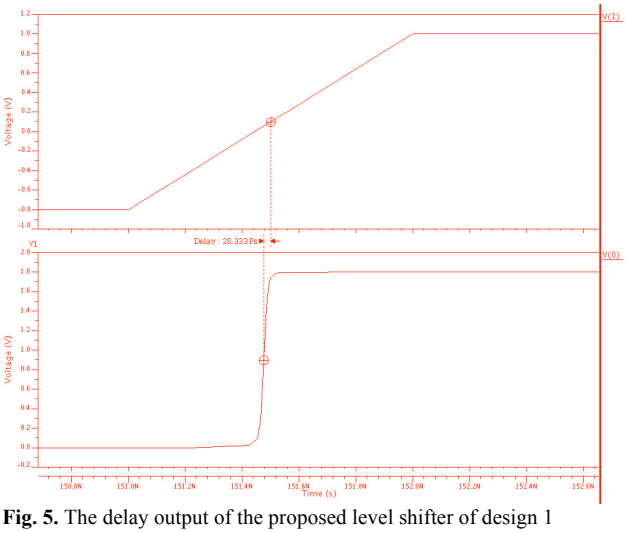

Fig. 5. The delay output of the proposed level shifter of design 1

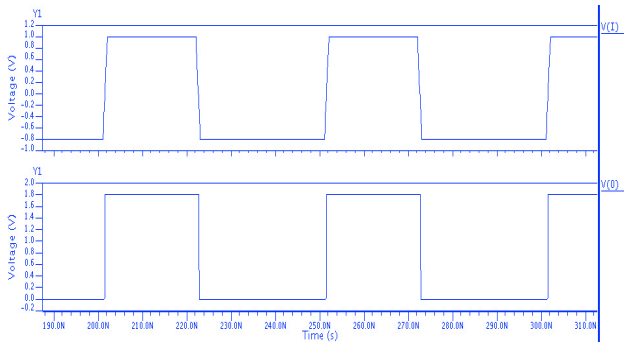

Fig. 6. The voltage conversion of the proposed level shifter of design 2

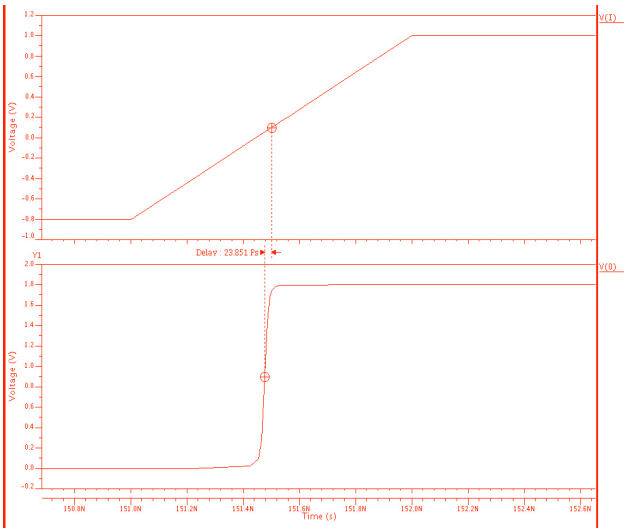

Fig. 7. The delay output of the proposed level shifter of design 2

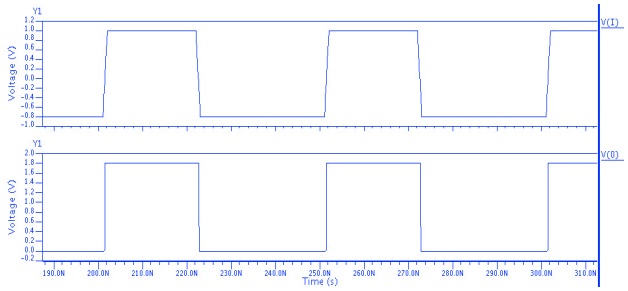

Fig. 8. The voltage conversion of the proposed level shifter of design 3

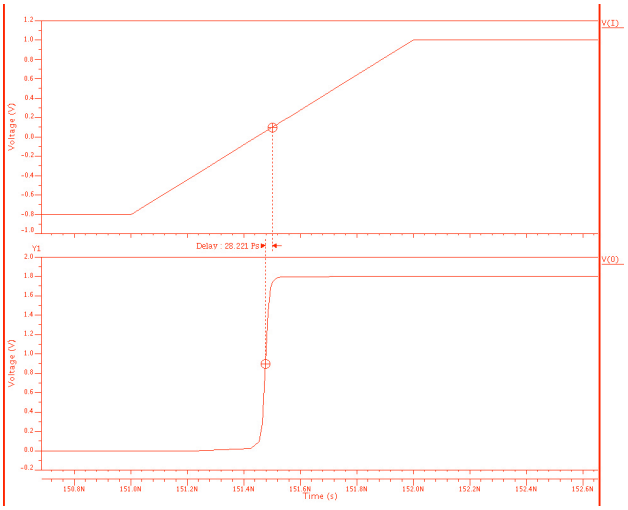

Fig. 9. The delay output of the proposed level shifter of design 3

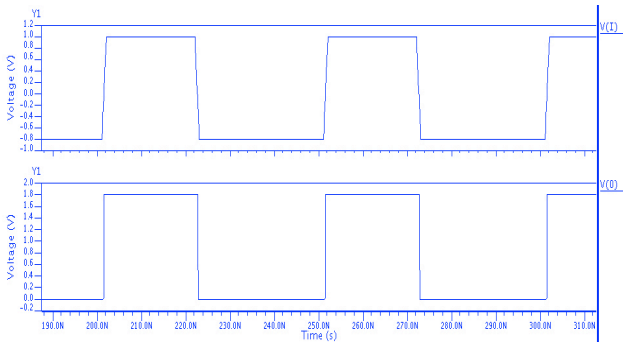

Fig. 10. The voltage conversion of the proposed level shifter of design 4

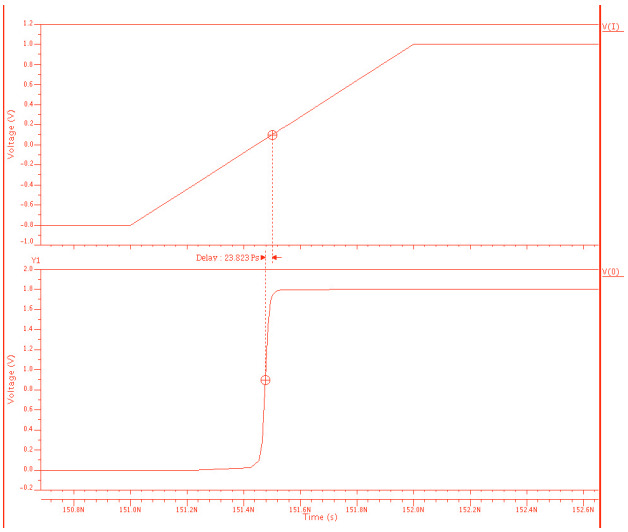

Fig. 11. The delay output of the proposed level shifter of design 4

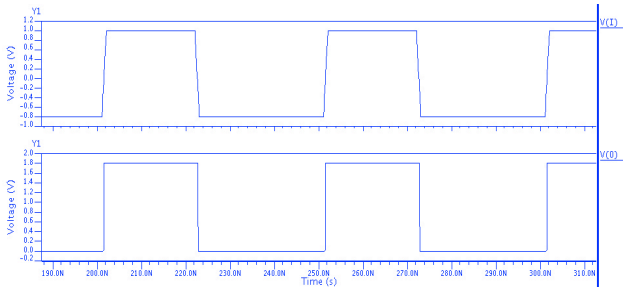

Fig. 12. The voltage conversion of the proposed level shifter of design 5

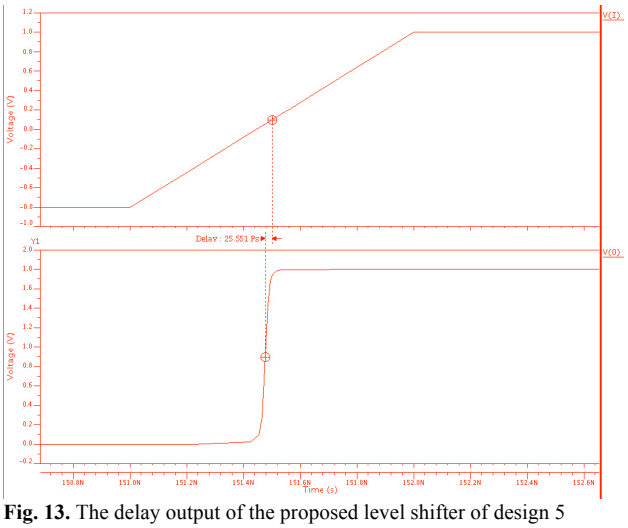

Fig. 13. The delay output of the proposed level shifter of design 5

Table 2 summarizes the amount of power dissipation and output delay for each of the five designs. The low power dissipation is obtained by designing both the (PMOS and NMOS) transistors with a same W/L ratio equal to 1µm/0.13µm. Having this W/L ratio of the transistors, the proposed LS circuit dissipates 0.1449 nW power. Moreover, second lowest delay of 25.551 ps is achieved in this design (design 5). Though design 2 managed to achieve the lowest delay but it has a high power consumption of 1.98 nW compare to design 5. Therefore, design 5 is the most acceptable among the five designs presented here. The results described in table 2 shows that application of transistor sizing is able to reduce the power dissipation and delay the output of the level shifter. The layout of the proposed level shifter circuit with a W/L ratio of all transistors equal to 1.0µm/0.13 µm has been designed using Mentor Graphics design kit and Silterra 0.13µm process technology. The layout of the proposed circuit is illustrated in figure 14. The measured area of the designed layout is only 17.36× 14.560 μm^2.

Table 2. Simulation results of the proposed level shifter circuit

Design No.	Design (W/L)	V_I (V)	Power dissipation (nW)	Delay (ps)
1	PMOS 2.0µ/0.13µm NMOS 2.0µ/0.13µm	1	3.5292	28.333
2	PMOS 2.0µ/0.13µm NMOS 1.4µ/0.13µm	1	1.9800	23.851
3	PMOS 1.4µ/0.13µm NMOS 1.4µ/0.13µm	1	2.6722	28.221
4	PMOS 1.4µ/0.13µm NMOS 1.0µ/0.13µm	1	0.9142326	23.823
5	PMOS 1.0µ/0.13µm NMOS 1.0µ/0.13µm	1	0.1449126	25.551

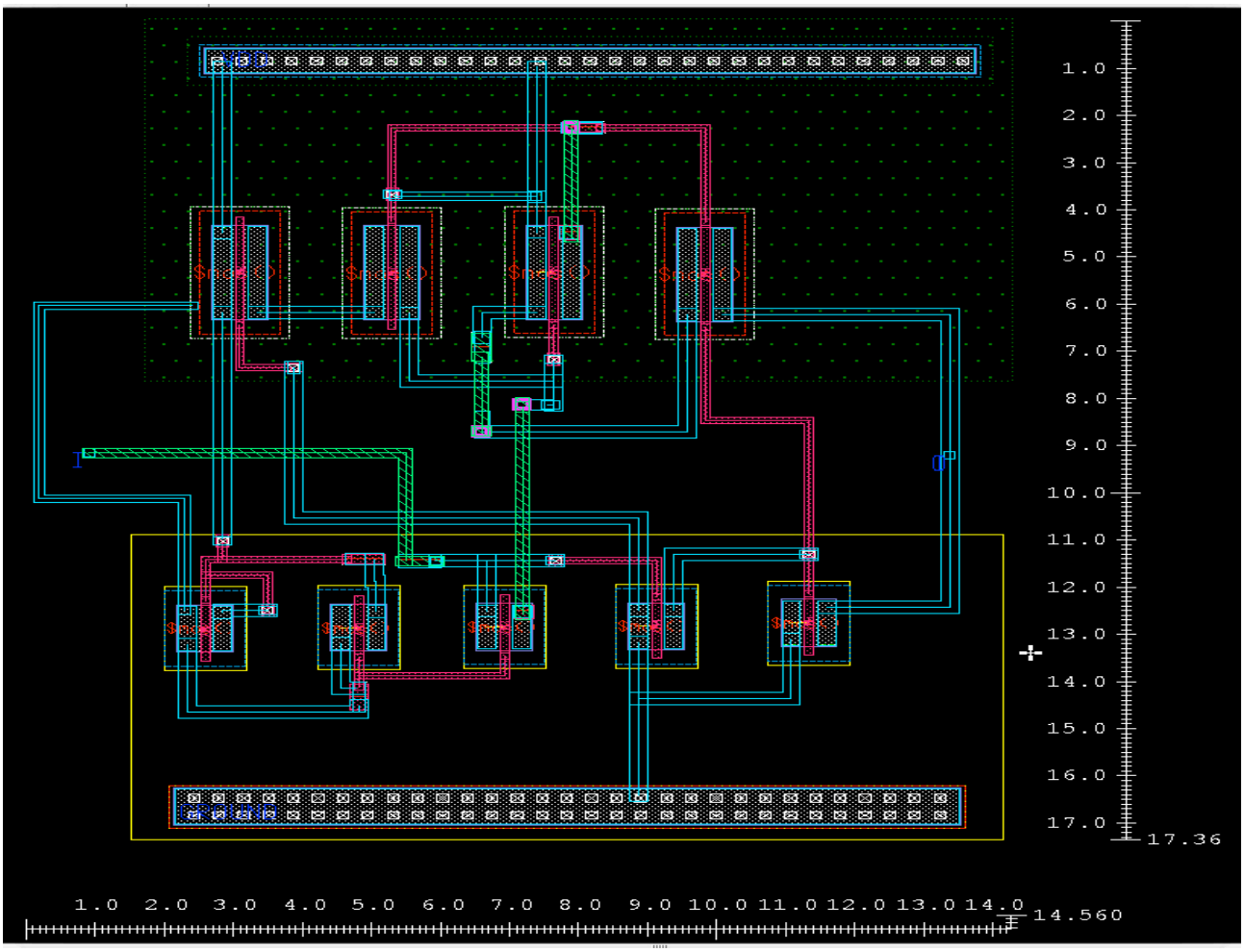

Fig. 14. The layout of the proposed level shifter circuit

Table 3 represents a comparison of performance results obtained in this research and those obtained in previous researches. From table 3, it is clear that both the power dissipation and output delay of the proposed circuit are many folds less than those for shifter circuits presented in both [9] and [23]. Similarly, the achieved power dissipation in this research is slightly lower while the output delay is

approximately 19×10^6 times smaller. Only the level shifter circuit presented in [21] consumes approximately 0.015 nW power less than the proposed level shifter which is a very insignificant amount. Nevertheless, the proposed level shifter circuit is approximately 1330 times faster compared to the level shifter circuit presented in [21]. Thus, from this comparison, it is evident that the designed level shifter circuit in this research marks a significant improvement in terms of operation speed and power dissipation of level shifter circuits.

Table 3. Performance summary of proposed LS circuit compared to other designs.

Publications year and reference	This work	[23] 2015	[21] 2014	[9] 2010
CMOS process µm	0.13	0.09	0.18	0.09
Type	Single supply voltage	Multiple supply voltage	Comparator	Latch
VDD independence	Yes	Yes	Yes	No
Power dissipation (nW)	0.1449	8.7	0.13	6.6
Delay(s)	25.55p	16.6n	30n	18.4n

4. Conclusion

In this article an enhanced level shifter circuit has been reported to meet the current demand of low power consumption and low delay operation. The proposed LS supports a wide range of voltage conversion and it reaches high-speed performance. The post layout simulation result shows that it is able to convert the 1 V input signal into 1.8V output voltage signal. Moreover, the designed circuit has managed to achieve significant low power dissipation of only 0.1449 nW and low delay output of 25.55ps. The designed LS is suitable for memory circuits of low power applications and can be widely used in different electronic devices to form efficient SoCs.

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