Journal of Engineering Science and Technology Review 10 (2) (2017) 220- 232

Research Article

JOURNAL OF
Engineering Science and Technology Review

www.jestr.org

Design of 16 Bit Vedic Multiplier Using Semi-Custom and Full Custom Approach

K. Nehru* and T.T.Linju

Institute of Aeronautical Engineering, Department of ECE, Hyderabad

Received 4 May 2016; Accepted 2 April 2017

Abstract

The Digital processor requires high speed and low power multiplier. This thesis is devoted to the design of vedic multiplier using semi-custom and full custom approach. The vedic multiplier is a specimen of interest because of its modular design where smaller blocks can be used for to design the bigger ones. Though the adders in the multiplier suffers from the carry propagation delay.So we incorporate a different kinds of adders and the performance was determined by the trade-offs between power delay and area parameters. The vedic mathematics algorithms like urdhvatiryakbhyam were used in the realization of the Vedic multiplier.The Semi-custom and Full custom approaches are utilized in designing the vedic multiplier.The Vedic multiplier was implemented in FARADAYS 180nm as well as FARADAYS 65nm technology for all the design corners in the semi-custom approach.In the Full custom approach we use Tanner EDA for schematic entry and simulation.

Keywords: CSLA, low-power, urdhvatiryakbhyam, VLSI.

1. Introduction

Multipliers is most commonly used in most of the digital signal processing applications. But the multiplication involves lot of computations such as partial product generation and shift and addtion of partial products.The moore's law states that the no.of transistor doubles approximately every two years.As the transistor density increases the power consumption of the digital IC became a major consideration for the designers. The dynamic power disipation is influenced by the frequency of operation,switching capacitance,supply voltage and activity factor.More over there is always a trade off between the speed, power and hardware utilised. Several algorithms were proposed in order to make the multiplication effective.In this paper we propose a multiplier design using vedic mathematics algorithm Urdhva tiryakbhyam (vertical and crosswise algorithm). The vedic mathematics can simplify the computations and increases the speed of computation which in turn increases the speed. More over the vedic multiplier has modular architecture than the other multipliers [1].

But the ripple carry adders (RCA) used in the vedic multiplier suffers from propagation delay. So we replace some other adders like carry skip adder, carry look ahead adder and carry select adder and analyse the performance in terms of power,delay and area. The use of carry select adder (CSLA) may help the multiplier to work faster, but at the cost of excess hardware almost twice that of ripple carry adder. Moreover the use of multiplexers increases the area of the digital ICs. So the optimisation of carry select adder may be useful in optimising the carry select adder. The use of add one circuit instead of a ripple carry adder block with carry one was a good option [4]. But this design is penalised by the delay factor. So in our design we use binary to excess 1 (BEC) circuit in order to make the multiplier to consume less power.

2. Architecture of Vedic Multiplier

This multiplier uses the vedic mathematics algorithm urdhvatiryakbhyam (vertical and crosswise algorithm) [1].Let see the illustration of using this algorithm.

2.1. 2x2 Multiplier

Let's take multiplication of 2 bit inputs A1A0 and B1B0.

In vedic method, P0 is vertical product of bit A0 and B0, P1 is addition of crosswise bit multiplication i.e. A1 & B0 and A0 and B1, and P2 is again vertical product of bits A1 and B1 with the carry generated, if any, from the previous addition during P1. P3 output is nothing but carry generated during P2 calculation. This module is known as 2x2 multiplier block.

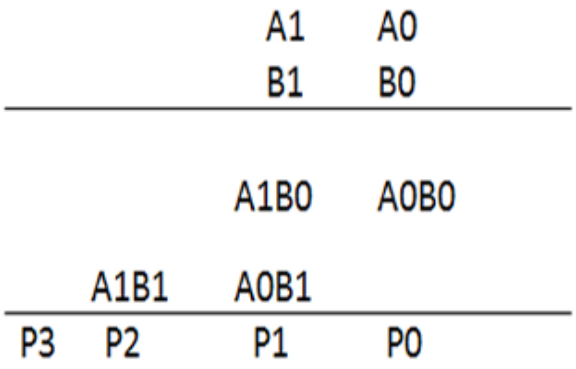


Fig. 1. 2x2 Multiplication algorithm

*E-mail address: nnehruk@gmail.com

2.2. 4x4 Multiplication

For multiplication of higher order bits, little modification is required. Let A3A2A1A0 and B3B2B1B0, the output for the multiplication results in P7P6P5P4P3P2P1P0. Block diagram of 4x4 vedic multiplier is given in Fig.2.

$$\begin{array}{l} A_3A_2\ \ A_1A_0 \\ \text{X}\ B_3B_2\ \ B_1B_0 \\ \text{----------} \end{array}$$

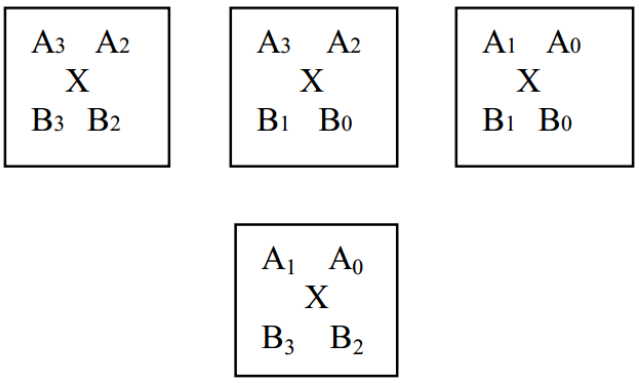


Fig. 2. 4x4 Multiplier block diagram

Each of the blocks denoted as square boxes in the above figure are 2x2 multipliers. On applying the algorithm the least bits A1A0 and B1B0 forms the first block, and the crosswise multiplication of the least bits and most bits A3A2 with B1B0 and A1A0 with B3B2 forms the second and third blocks and the vertical multiplication of the most bits A3A2 and B3B2. The results of these blocks is given as

A_3A_2	A_3A_2	A_1A_0	A_1A_0
B_3B_2	B_1B_0	B_3B_2	B_1B_0
----------	----------	----------	---------
$S_{33}S_{32}S_{31}S_{30}$	$S_{23}S_{22}S_{21}S_{20}$	$S_{13}S_{12}S_{11}S_{10}$	$S_{03}S_{02}S_{01}S_{00}$

The result is obtained by adding S13S12S11S10 with S23S22S21S20. Now this sum is added with Most Significant two bits of first block andLeast Significant two bits of fourth block like S31S30S03S02.

$$\begin{array}{lcccc} S_{33}S_{32} & 0 & 0 & S_{03} & S_{02} \\ & S_{23} & S_{22} & S_{21} & S_{20} \\ & S_{13} & S_{12} & S_{11} & S_{10} \\ & S_{31} & S_{30} & 0 & 0 \\ \hline P_7P_6 & P_5 & P_4 & P_3 & P_2 \end{array} \quad S_{01}S_{02} \quad P_1P_0$$

2.3. 8x8 Multiplication

For 8 bit multiplicand A is splitted into pair of four bits AH-AL. Similarly multiplier B can be decomposed into BH-BL. The urdhavatiryakbhyam algorithm is applied. The outputs of 4X4 bit multipliers are added accordingly to obtain the final product. Thus, we require two adders in order to perform the multiplication. The basic building block of 8x8 bits Vedic multiplier is 4x4 bits multiplier. For 8x8 bits multiplier the 4x4 bits multiplier units has been used as basic components and for 4x4 bit vedic multiplier the basic block is 2x2 multiplier. Thus it forms a modular architecture. The sample calculation is given below

For example

	1111	1111	
	0000	1001	
0000	0000	0000	0111
	1000	0111	
	0000	1000	
0000	1000	1111	0111

255 x 9 = 2295

Fig. 3. Sample Calculation of 8x8 multiplication

3. Architecture of Existing 16 Bit Vedic Multiplier

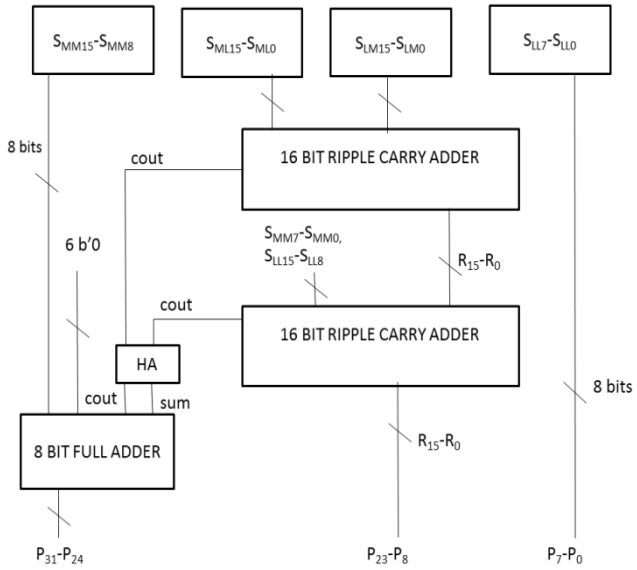


Fig. 4. Architecture of Vedic multiplier

The 16x16 bit multiplier is built using 8x8 bit blocks. The 16 bit multiplicand A can is divided into pair of 8 bits AH-AL. Similarly multiplier B is divided into BH-BL. The outputs of 8x8 bit multipliers are added accordingly to obtain the 32 bits final product. Two 16 bit ripple carry adders are used for the addition of partial products. The ripple carry adder is simplest form among adder families. The least hardware requirements and less power consumption make the adder attractive for low power applications. The problem in using the ripple carry adders are they suffer from carry propagation delay. The carry will be available only after passing through all the full adder blocks. We cannot entertain such delay in communication systems where high speed digital signal processing is required.

5. Proposed Vedic Multipliers

In the existing 16x16 multiplier architecture the generation of the partial outputs from the low order multipliers occurs concurrently.But the large ripple carry adders will contribute to larger delays as the size of the multiplier increases.So, several architectures are proposed by replacing the 16 bit RCA with some other adders and analyse their performance with power, delay and area attributes.

5.1 Vedic Multiplier Using Carry Skip Adder

In the existing multiplier, the ripple carry adder block is replaced by the carry skip adder.

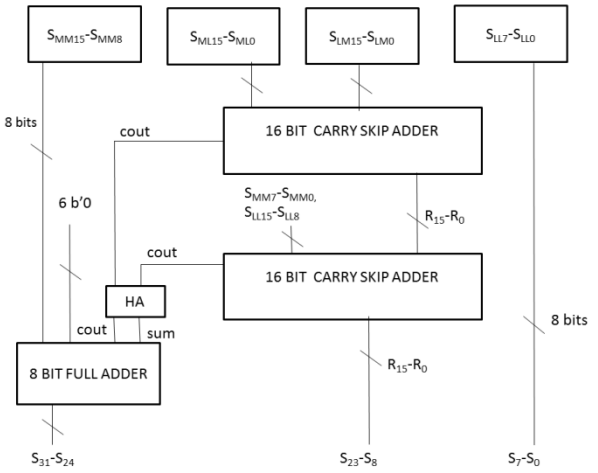


Fig. 5. Vedic Multiplier using Carry skip adder

The two bit streams to be added are divided into blocks of equal length say 16 bits are divided into two eight bit streams. The carry is skipped through the stages based on un-equivalence condition. This is done by Exclusive OR ing each individual block which leads to comparison string which is subjected to AND operation within itself. If for each cell in the block Ai ≠ Bi then we say that a carry can skip over the block otherwise if Ai = Bi we shall say that the carry must be generated in the block. This operation is accomplised by the use of multiplexers.

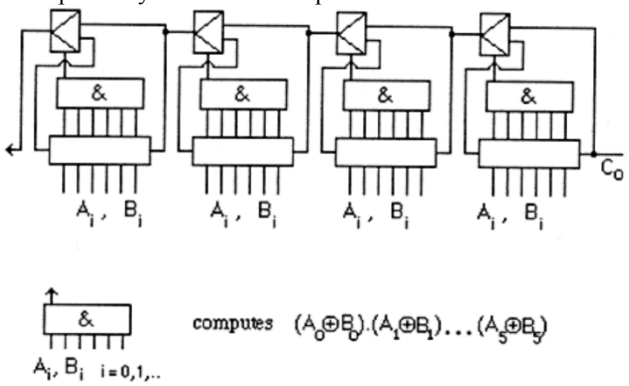


Fig. 6. Carry Skip Adder

5.2. Vedic Multiplier using Carry Look Ahead Adder

In the existing multiplier,the RCA block is replaced by the carry look ahead adder.

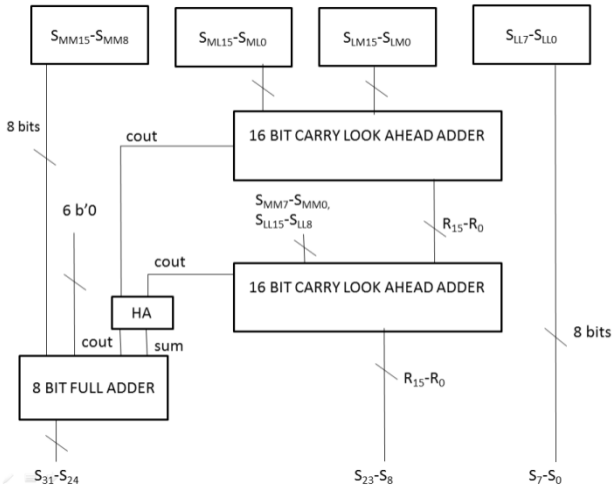


Fig. 7. Vedic multiplier using Carry Look Ahead adder

Carry look aheadadder produces carry bit faster due to carry bits generated in parallel by an additional circuit.This technique uses carry bypass logic chain which has generate and propagate functions to speed up the carry propagation. The expressions for carry generation are

Propagate function, $p_i = a_i + b_i$ (1)

Generate function, $g_i = a_i b_i$ (2)

Sum $s_i = p_i \wedge c_i$ (3)

Carry $c_{i+1} = g_i + p_i c_i$ (4)

But the additional circuitry is achieved at the cost of extra hardware and power.Moreover, when the no.of bits increases the complexity of implemeting the carry look ahead adder is cumbersome. So it is not perferable to use conventional carry look ahead adder, rather we could break the circuit into small blocks and low order adders can be used.

5.3. Vedic Multiplier using Carry Select Adder

In the existing multiplier, the RCA block is replaced by the carry select adder.

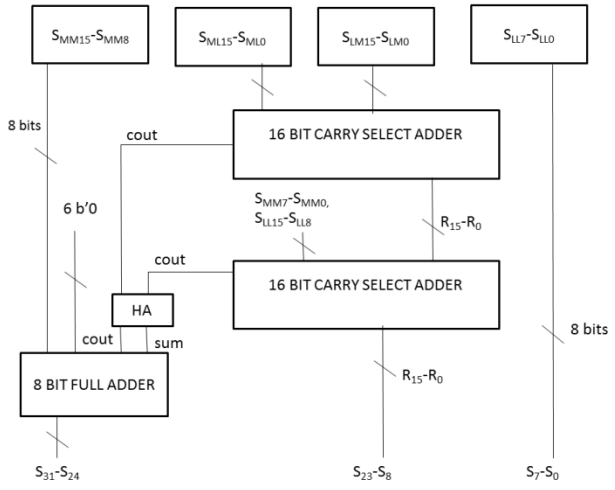


Fig. 8. Vedic multiplier using Carry select adder

The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stages. In carry-select adders both sum and carry bits are calculated for the two alternatives: carry "0" and "1". Once the carry-in is fired, the correct computation is chosen using multiplexers to produce the desired output.Therefore instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed.

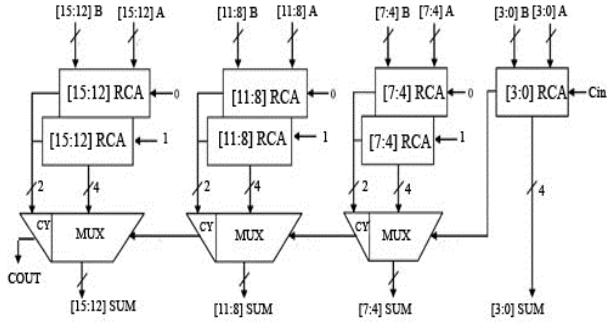


Fig. 9. Carry Select adder

The use of carry select adder increases the hardware thereby more power consumtion which is twice that of rippe carry adder.The use of multiplexer increases the chip area.But consierable increase in the speed is achieved. So, optimisation of the carry select adder can be useful in increasing the speed of the mutiplier speed.

5.4. Vedic Multiplier using Modified Carry Select Adder with BEC

In the existing multiplier, the RCA block is replaced by the modified carry select adder with BEC (Binary to Excess-1).

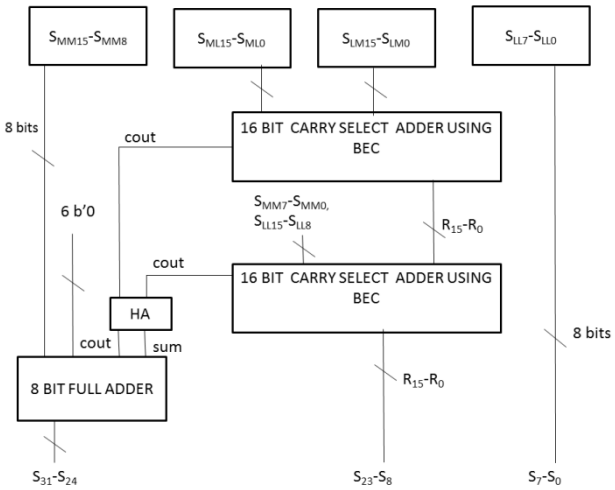


Fig. 10. Vedic Multiplier using Carry Select adder with BEC

In the carry select adder the there are two stages of ripple carry adder with carry 0 and carry 1, once the carry is delivered from the previous stage, then the output is selected based on the input carry. Comparing the results from the ripple carrystages with $c_{in}0$ andc_{in} 1. The outputs of the ripple carry stage with c_{in} value 1 will be one excess than that of the ripple carry stage with c_{in} value 0. So, there is an option of Binary to Excess – 1 (BEC-1) instead of the ripple carry block with c_{in} 1. The function table of the 4 bit BEC is given in Table1.

Table 1.BEC Truth Table

Binary (B)	BEC-1 (X)
0000	0001
0001	0010
0010	0011
…	…
1110	1111
1111	xxxx

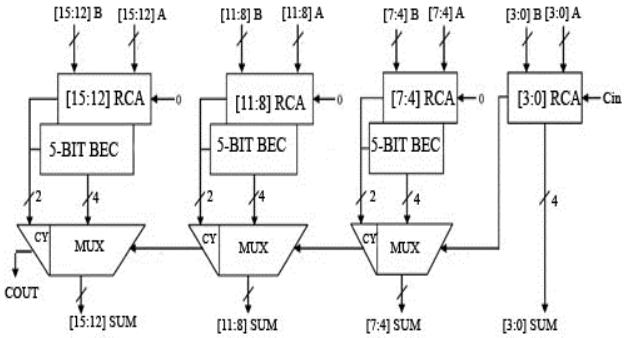


Fig. 11. Modified Carry Select adder

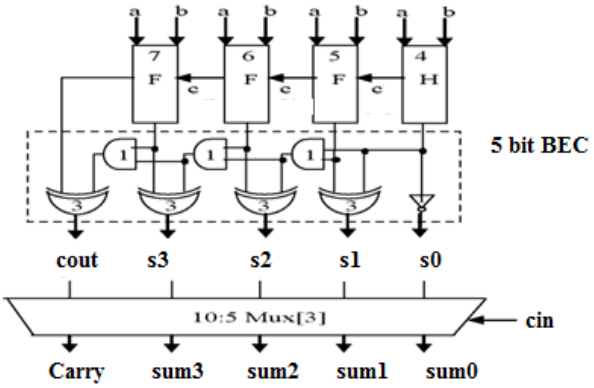


Fig. 12. 5-bit Binary to Excess 1 block

5.4. Vedic Multiplier using SQRT Carry Select adder

In the existing Multiplier, the RCA block is replaced by the square root carry select adder (SQRT CSLA) a variant of carry select adder.

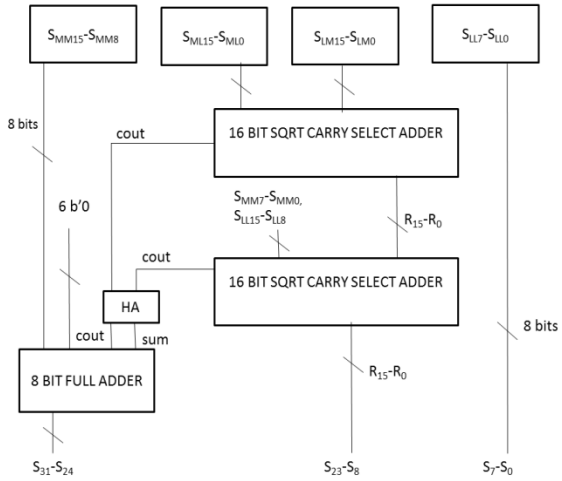


Fig. 13. Vedic multiplier using SQRT Carry select adder

The square root carry select adder is a variant of the conventional carry select adder where it has a balanced delay than the CSLA. The SQRT CSLA differs from the CSLA in a way that the RCA blocks are of different sizes. The smaller blocks were placed first and the size increases as towards the higher order bits.

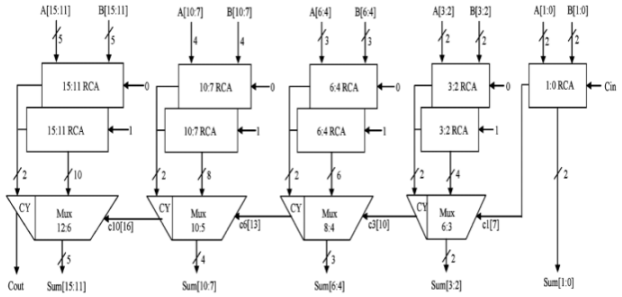


Fig. 14. SQRT Carry Select adder

5.6. Vedic Multiplier using SQRT Carry Select Adder with BEC

In the existing multiplier, the RCA block is replaced by the modified square root carry select adder using BEC.

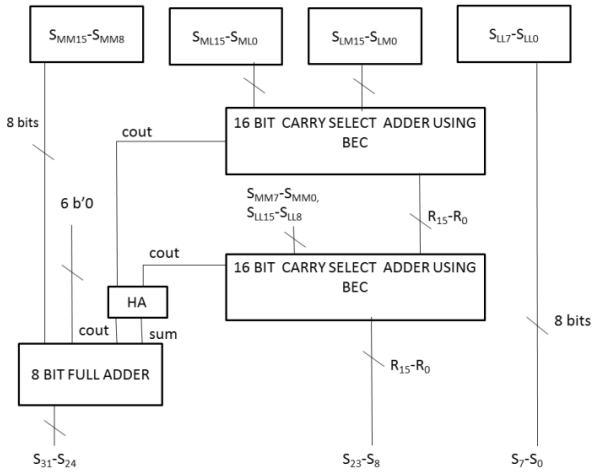


Fig. 15. Vedic Multiplier using SQRT Carry Select adder with BEC

In the square root carry select adder the variable sizes of parallel RCA blocks with cin = '0' and cin = '1' are used. In modified SQRT CSLA, the RCA block with cin = '1' block is replaced by corresponding BEC group. The 2 bit,3bit,4bit, 5bit RCA blocks with cin=1 are replaced with 3bit,4bit, 5bit,6bit BEC blocks respectively.

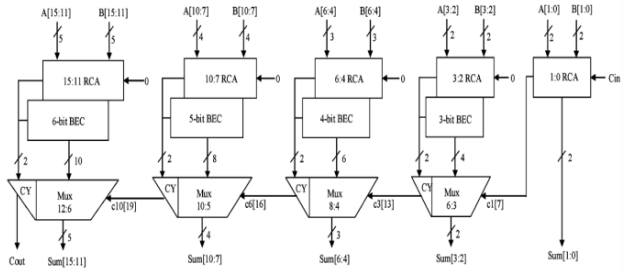


Fig. 16. Modified SQRT Carry Select adder with BEC

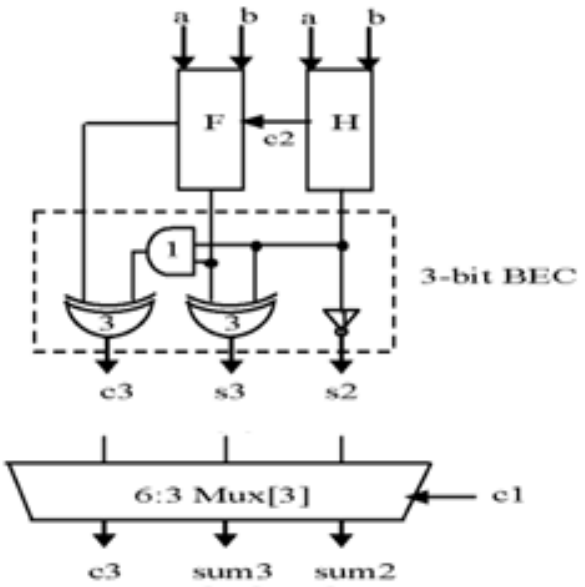


Fig. 17. 3-bit BEC

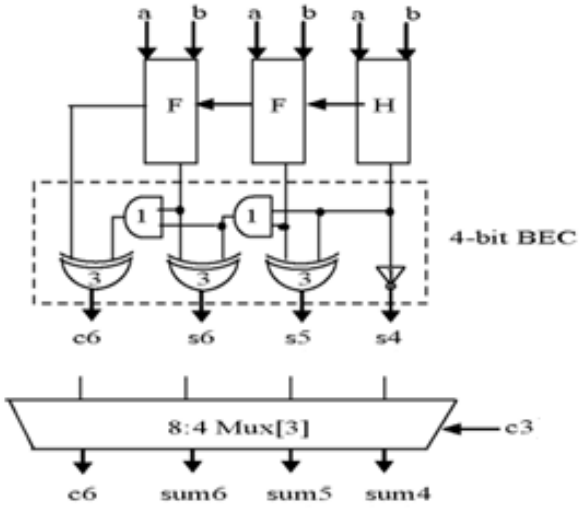


Fig. 18. 4-bit BEC

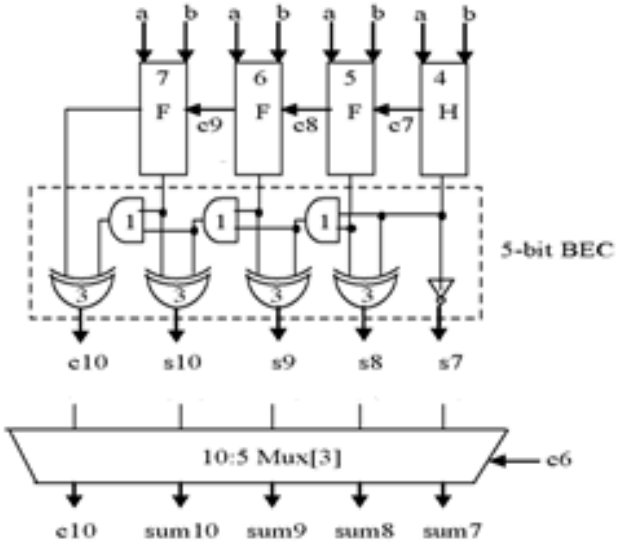


Fig. 19. 5-bit BEC

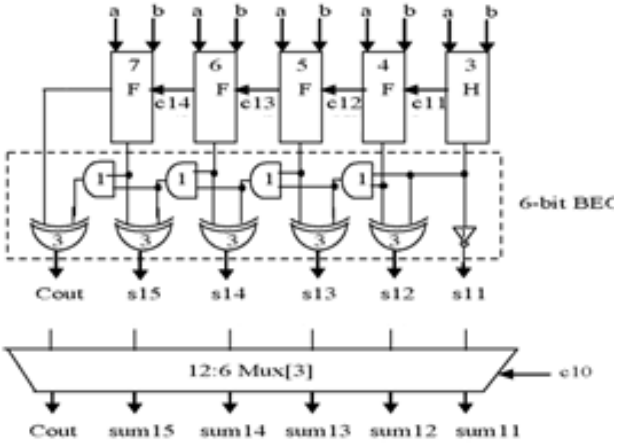


Fig. 20. 6-bit BEC

5. Implementation

For the implementation we took both semi-custom and full custom approaches. For the semi-custom approach the synopsis design compiler was used for synthesis and cadence SoCencounter was used for layout design.All the existing multipliers and designed using verilog HDL using dataflow and behavioural modelling.The multipliers were implemented in both Faradays 180nm as well as 65nm technology for all the process corners. For full custom approach we use tanner EDA S-edit for schematic entry and T-SPICE for circuit simulation.

6. Results and Discussion

Table 2.Results of Fast-Fast design corner (Faradays 180nm)

SLOW-SLOW DESIGN CORNER				
	POWER mW	DELAY nS	AREA μm^2	POWER DELAY PRODUCT (10^{-12})
MUL_RCA	3.2173	2.23	10448.37	7.174579
MUL_CLA	3.2225	2.21	10435.82	7.121575
MUL_CSKA	3.2819	2.45	10518.93	8.040655
MUL_CSLA	5.4879	2.2	13077.12	12.07338
MUL_CSLA_BEC	4.5106	2.22	12098.69	10.01353
MUL_SQRTCSLA	4.1358	2.16	11334.29	8.933328
MUL_SQRTCSLA_BEC	3.8093	2.17	11003.44	8.266181

In the above table, The results of all the multiplier designs using faradays 180nm technology Fast- Fast design corner is tabulated. As far as power is concerned the multiplier with ripple carry adder is the best option but it has considerable amount of delay than all the other designs. The delay in carry select adder was good but it has very high power consumption. But the multiplier designed with modified carry select adder using BEC has the less power consumption than the multiplier with carry select adder but it has a bit more delay. The variant multiplier using square root carry select adder has less power and delay than the carry select adder. But the modified square root carry select adder looks promising as it has less delay and the power consumption was also bit more than the ripple carry adder.

Table 3. Results of Slow-Slow design corner (Faradays 180nm)

SLOW-SLOW DESIGN CORNER				
	POWER mW	**DELAY nS**	**AREA μm^2**	**POWER DELAY PRODUCT (10^{-12})**
MUL_RCA	1.9989	6.3	10448.37	12.59307
MUL_CLA	2.0039	6.28	10435.82	12.58449
MUL_CSKA	2.0378	6.95	10518.93	14.16271
MUL_CSLA	3.3408	6.22	13077.12	20.77978
MUL_CSLA_BEC	2.7594	6.34	12098.69	17.4946
MUL_SQRTCSLA	2.5342	6.12	11334.29	15.5093
MUL_SQRTCSLA_BEC	2.3443	6.18	11003.44	14.48777

In the above table, the results of all the multiplier designs using faradays 180nm technology Slow – Slow design corner is tabulated. The Slow – Slow design corner has less power than the Fast – Fast design corner designs but the delay hikes up to greater extent.Analysing the results the multiplier with ripple carry adder has less hardware components it has the least power but the delay is pretty high. Though the multiplier with carry select adder speeds up the multiplication it consumed more power. The proposed multiplier with modified carry select adder using BEC consumes less power than the multiplier with CSLA its delay is more than the multiplier with CSLA. The multiplier with SQRT CSLA is good with least delay to all the designs. The multiplier with modified SQRT CSLA is good with power less than multiplier with SQRT CSLA adder with multiplier with SQRT CSLA and few hundred micro watts more than the multiplier RCA adder.

Table 4. Comparisons of Typical-Typical design corner (Faradays 180nm)

TYPICAL-TYPICAL DESIGN CORNER				
	POWER mW	DELAY nS	AREA μm^2	POWER DELAY PRODUCT (10^{-12})
MUL_RCA	1.0508	2.84	4169.28	2.984272
MUL_CSKA	1.0324	2.87	4118.08	2.983636
MUL_CSLA	1.0752	3.22	4196.8	3.462144
MUL_CSLA BEC	1.7344	2.7	5247.07	4.68288
MUL_SQRTCSLA	1.443	2.91	4809.6	4.19913
MUL_SQRTCSLA BEC	1.345	2.72	4532.8	3.6584
MUL_RCA	1.231	2.85	4385.6	3.50835

In the above table, the results of all the multiplier designs using faradays 180nm technology Typical-Typical design corner is tabulated. The Typical–Typical corner intermediate between the Fast–Fast and Slow – Slow cornershavingdelayandpower in consideration.The trade-offs between the designs was same as the other design corners. Here also multiplier with multiplier with SQRT CSLA using BEC holds good trade-offs between power and delay.As far as area is concerned the area for the designs is same for all the design corners. The multiplier with carry select adder has more area because of its increased hardware and multiplier with ripple carry adder has least area.

Table 5. Comparisons of Fast-Fast design corner (Faradays 65nm)

FAST-FAST DESIGN CORNER				
	POWER mW	DELAY nS	AREA μm^2	POWER DELAY PRODUCT (10^{-12})
MUL_RCA	1.4288	1.77	4169.28	2.528976
MUL_CLA	1.4018	1.79	4118.08	2.509222
MUL_CSKA	1.4605	2.01	4196.8	2.935605
MUL_CSLA	2.3511	1.66	5247.07	3.90282
MUL_CSLA_BEC	1.9549	1.79	4809.6	3.49927
MUL_SQRTCSLA	1.8274	1.7	4532.8	3.10658
MUL_SQRTCSLA_BEC	1.6703	1.76	4385.6	2.93972

In the above table, the results of all the multiplier designs using faradays 65 nm technology Fast- Fast design corner is tabulated. Considering the power is concerned the multiplier with ripple carry adder is the best option but it has considerable amount of delay than all the other designs. The delay in carry select adder was good but it has very high power consumption. But the multiplier designed with modified carry select adder using BEC has the less power consumption than the multiplier with carry select adder but it has a bit more delay. The variant multiplier using square root carry select adder has less power and delay than the carry select adder. But the delay in modified Square root carry select adder with BEC (1.76nS) has delay almost equal to ripple carry adder(1.77nS) but consumes more power than the ripple carry adder. So cannot afford such high hardware and power when a design with less hardware and power can offer the same performance.

Table 6. Comparisons of Slow-Slow design corner (Faradays 65nm)

SLOW-SLOW DESIGN CORNER				
	POWER mW	DELAY nS	AREA μm^2	POWER DELAY PRODUCT (10^{-12})
MUL_RCA	0.8231	4.97	4169.28	4.090807
MUL_CLA	0.8097	5.12	4118.08	4.145664
MUL_CSKA	0.8421	5.65	4196.8	4.757865
MUL_CSLA	1.3491	4.86	5247.04	6.55662
MUL_CSLA_BEC	1.1257	5.25	4809.6	5.90992
MUL_SQRTCSLA	1.0481	4.81	4532.8	5.04136
MUL_SQRTCSLA_BEC	0.9618	5.07	4385.6	4.87632

In the above table the results of all the multiplier designs are tabulated. The multiplier with ripple carry adder has least power delay product and looks very good best. Though the multiplier with carry select adder has least delay but power peaks up very high. The multiplier with modified carry select adder consumes less power than multiplier with carry select adder its delay is comparatively very high. The multiplier with modified SQRT CSLA has less delay than other carry select adders it has nominal increase in power than the ripple carry adder and so this design does hold good. But the multiplier with modified SQRT CSLA with BEC is considerable high in delay and power than multiplier with ripple carry adder it is not preferable for the slow-slow design corner of Faradays 65nm technology.

Table7. Comparisons of Typical-Typical design corner (Faradays65 nm)

TYPICAL-TYPICAL DESIGN CORNER				
	POWER mW	DELAY nS	AREA μm^2	POWER DELAY PRODUCT (10^{-12})
MUL_RCA	1.0508	2.84	4169.28	2.984272
MUL_CSKA	1.0324	2.87	4118.08	2.983636
MUL_CSLA	1.0752	3.22	4196.8	3.462144
MUL_CSLA BEC	1.7344	2.7	5247.07	4.68288
MUL_SQRTC SLA	1.443	2.91	4809.6	4.19913
MUL_SQRTC SLA BEC	1.345	2.72	4532.8	3.6584
MUL_RCA	1.231	2.85	4385.6	3.50835

On analysing the multiplier designs implemented in faradays 65nm technology typical-typical process corners. The multiplier with RCA is less power consuming and promising in delay when compared to other designs. But multiplier with carry look ahead adder also has good figures in terms of power and delay less than multiplier with RCA. Though multiplier with CSLA reduces the delay the power consumed is very high. The multiplier with CSLA BEC reduces the power than multiplier with CSLA but increases delay more than the multiplier with RCA. The multiplier with SQRT CSLA is also a good option when compared to power but the delay is almost equal to multiplier with RCA.

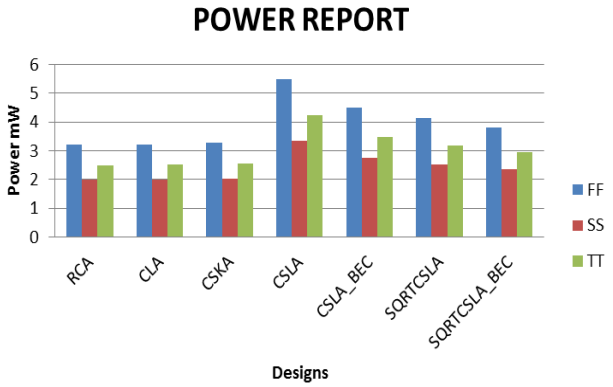


Fig. 21. Power Report (Faradays 180 nm)

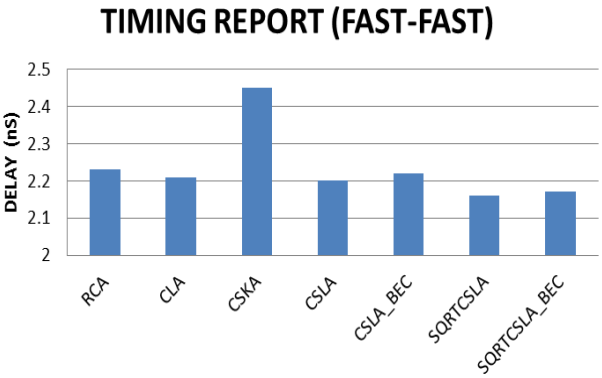


Fig. 22. Delay for Fast Fast design corner(Faradays 180 nm)

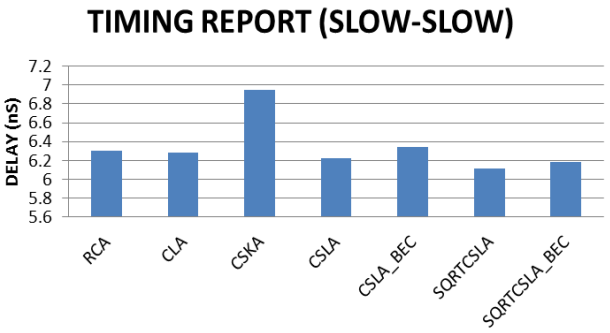


Fig. 23. DelayforSlow Slow design corner (Faradays 180 nm)

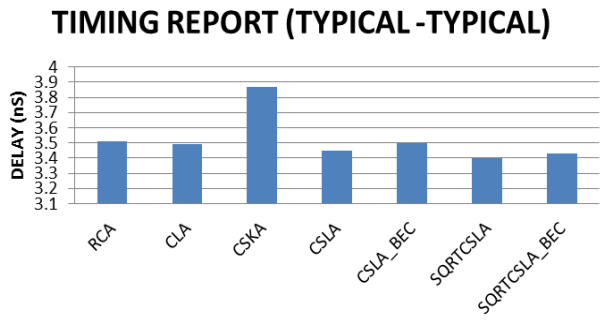


Fig. 24. Delay for TT design corner (Faradays 180 nm)

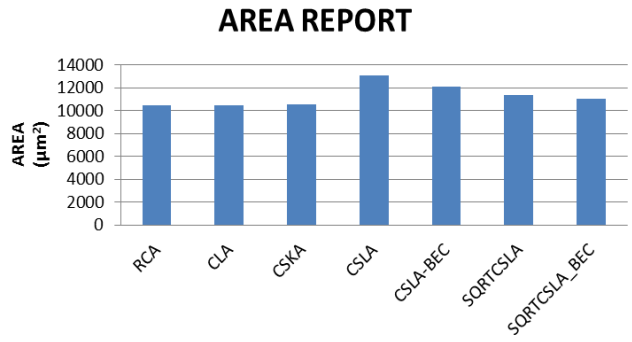


Fig. 25. Area report for all design corners

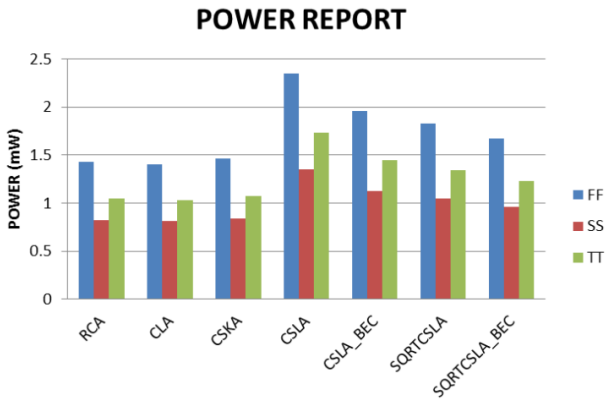


Fig. 26. Power report (Faradays 65 nm)

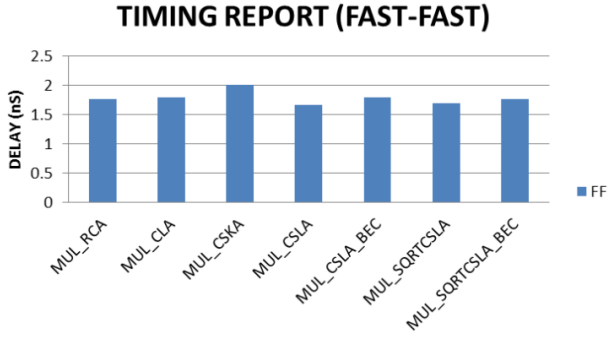


Fig. 27. Delay for Fast-Fast design corner (Faradays 65 nm)

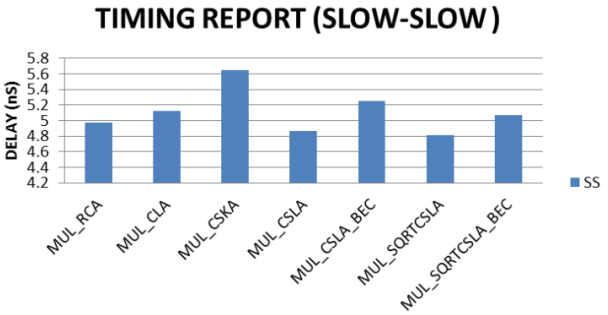


Fig. 28. Delay for Slow-Slow design corner (Faradays 65 nm)

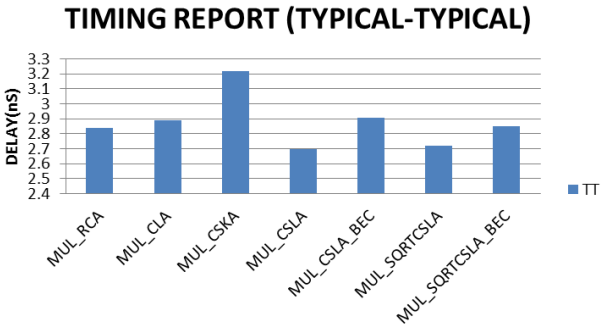


Fig. 29. Delay for Typical-Typical design corner (Faradays 65 nm)

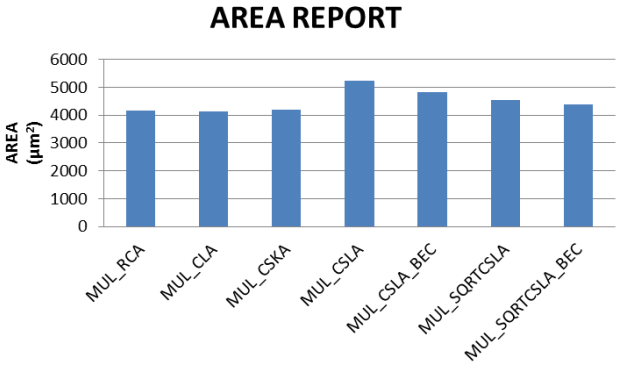


Fig. 30. Area Report (Faradays 65 nm)

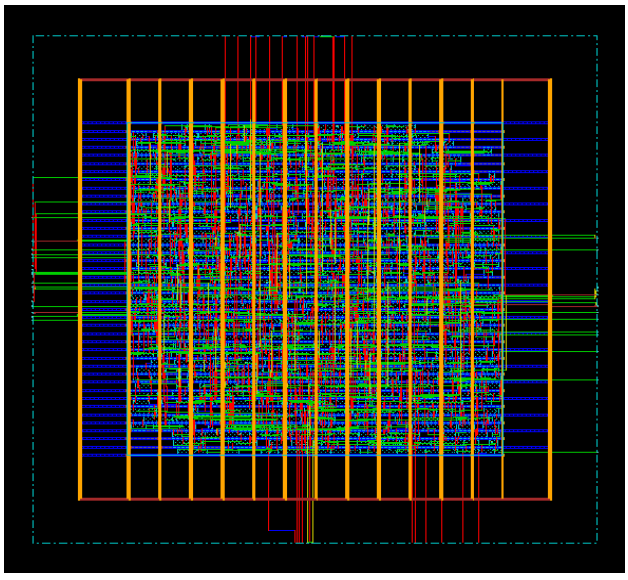


Fig. 31. Layout of Vedic multiplier using SQRT CSLA BEC (Faradays 180 nm FF)

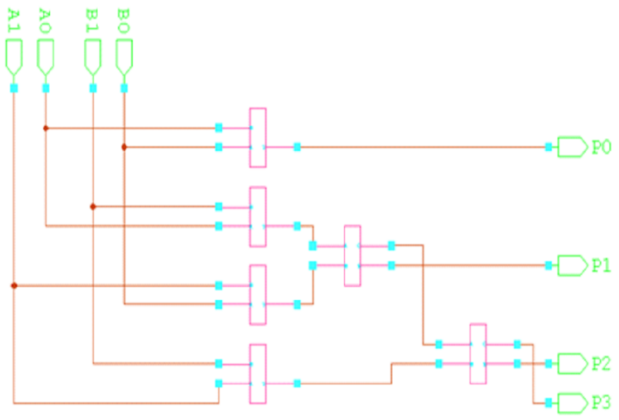


Fig. 32. Schematic of 2 bit Vedic multiplier

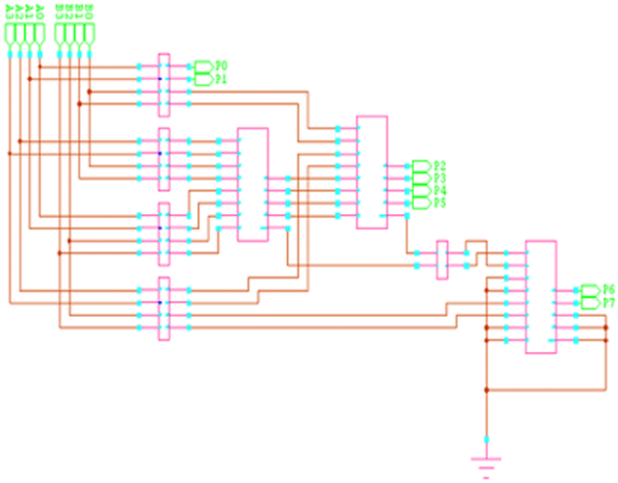


Fig. 33. Schematic of 4 bit Vedic multiplier

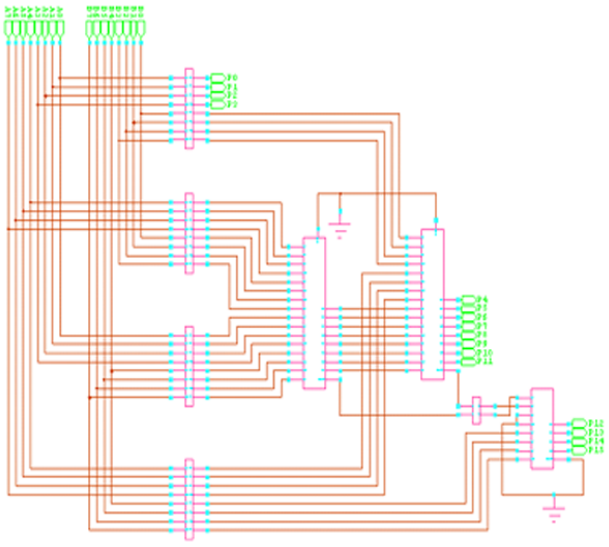


Fig. 34. Schematic of 8 bit Vedic multiplier

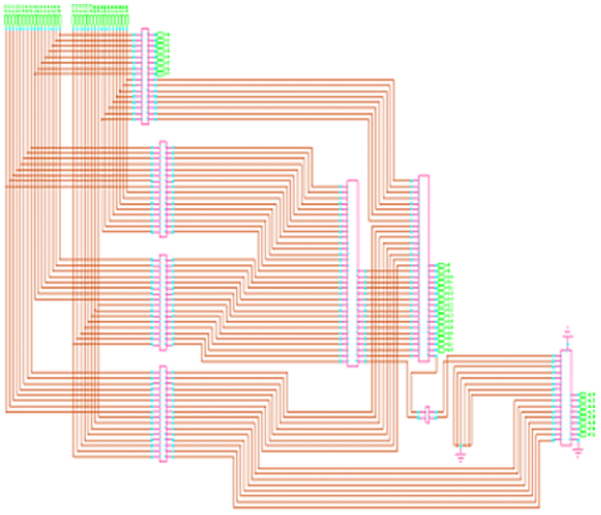


Fig. 35. Schematic of 16 bit Vedic Multiplier

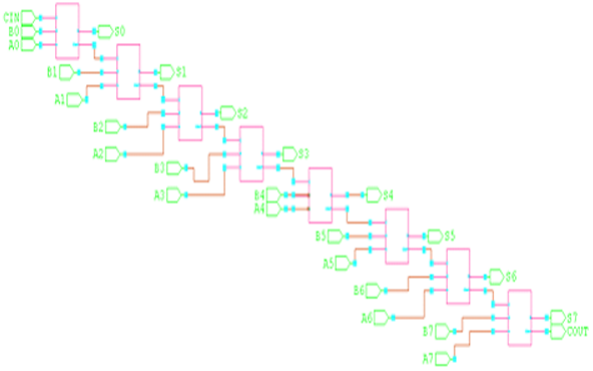


Fig. 36. Schematic of 8 bit Ripple Carry Adder

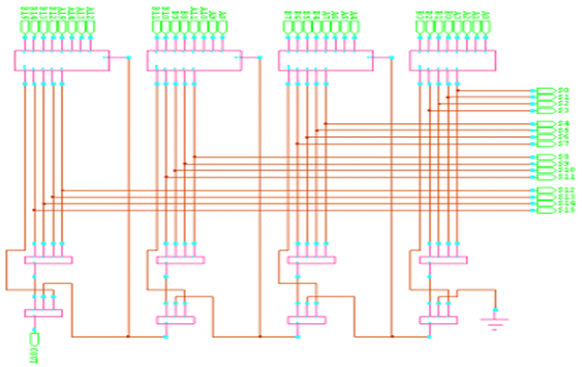
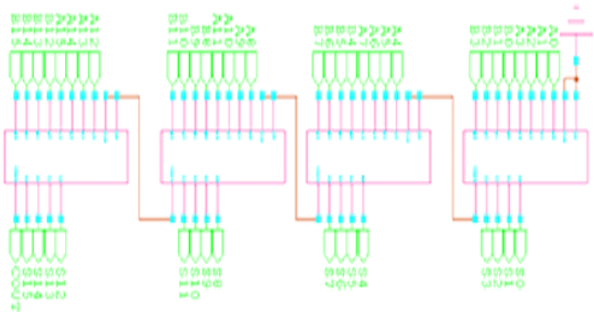


Fig. 37.Schematic of 16 bit Carry Skip adder



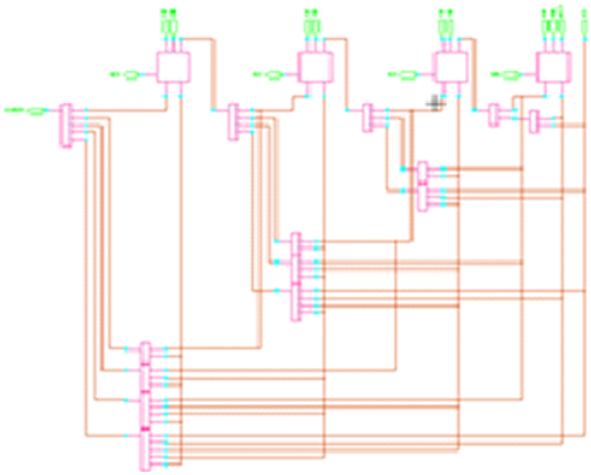


Fig. 38. Schematic of 16 bit Carry Look Ahead Adder

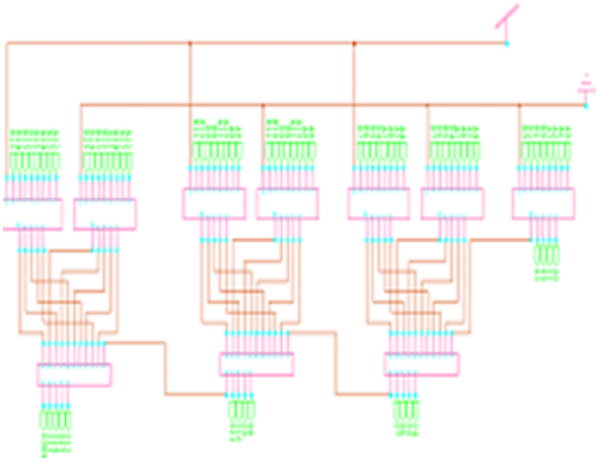


Fig. 39. Schematic of 16 bit Carry Select Adder

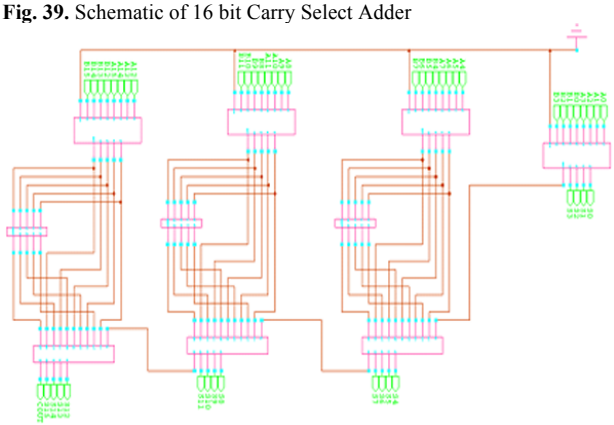


Fig. 40. Schematic of 16 bit Carry Select Adder using BEC

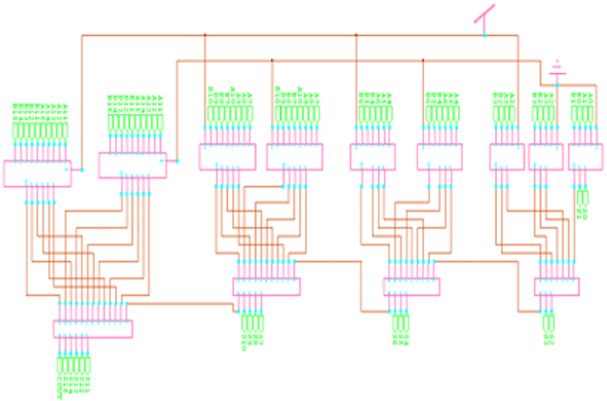


Fig. 41. Schematic of 16 bit Square root Carry Select adder

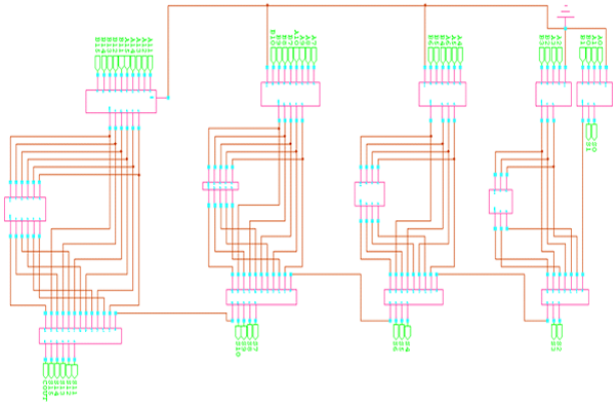


Fig. 42. Schematic of 16 bit Square root Carry Select Adder using BEC

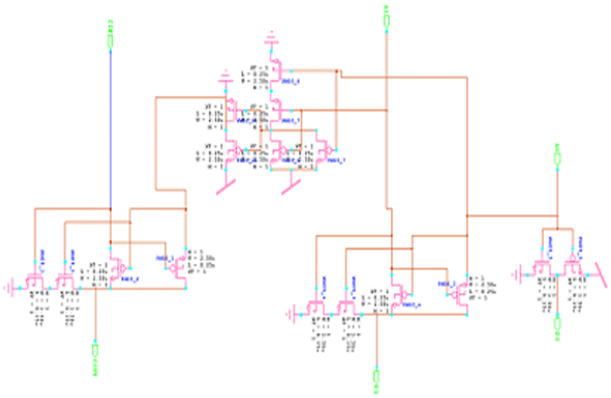


Fig. 43. Schematic of 3 bit BEC block

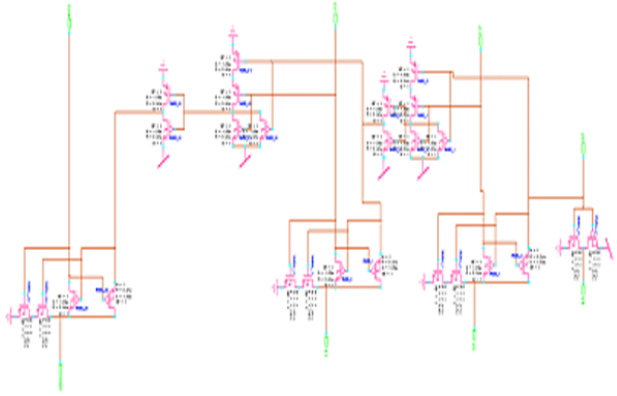


Fig. 44. Schematic of 4 bit BEC block

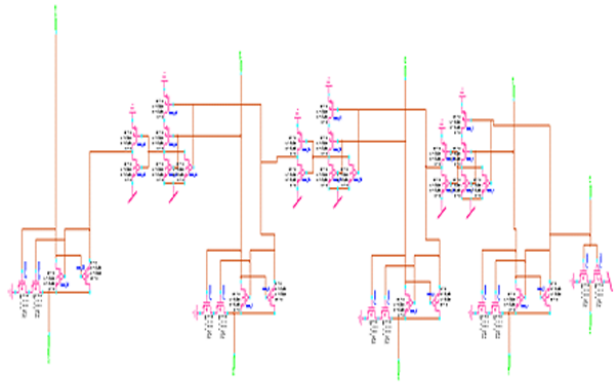


Fig. 45. Schematic of 5 bit BEC block

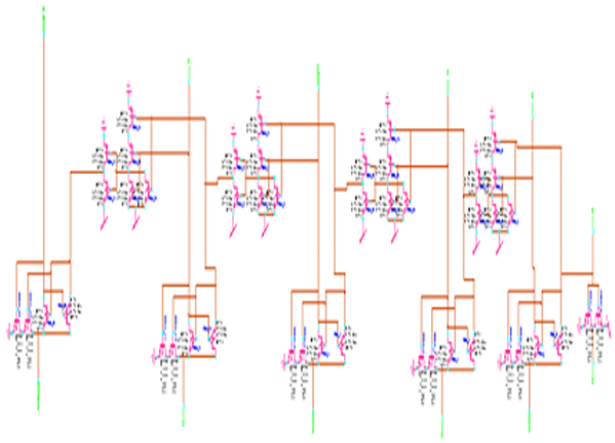
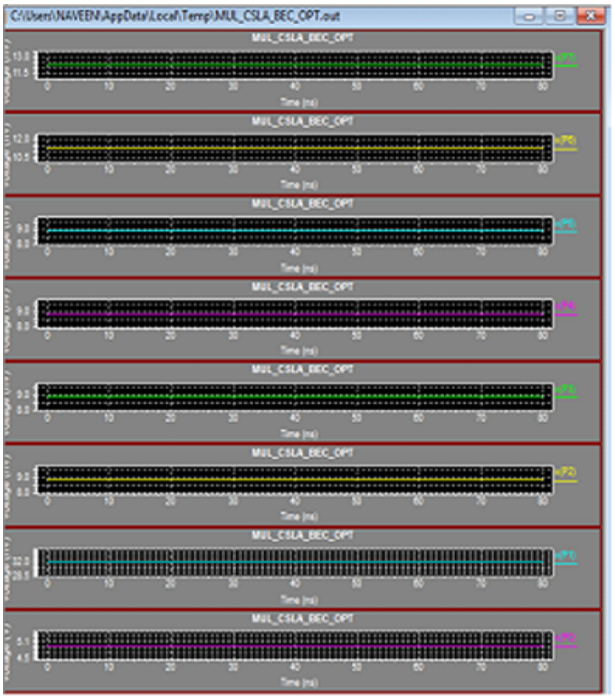


Fig. 46. Schematic of 6 bit BEC block



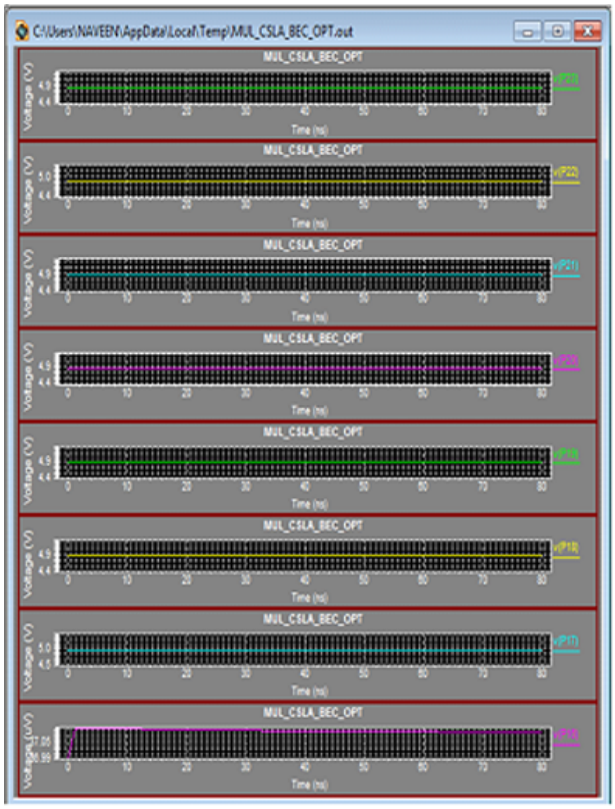


Fig. 47. Multiplier using Carry Select Adder with BEC outputs

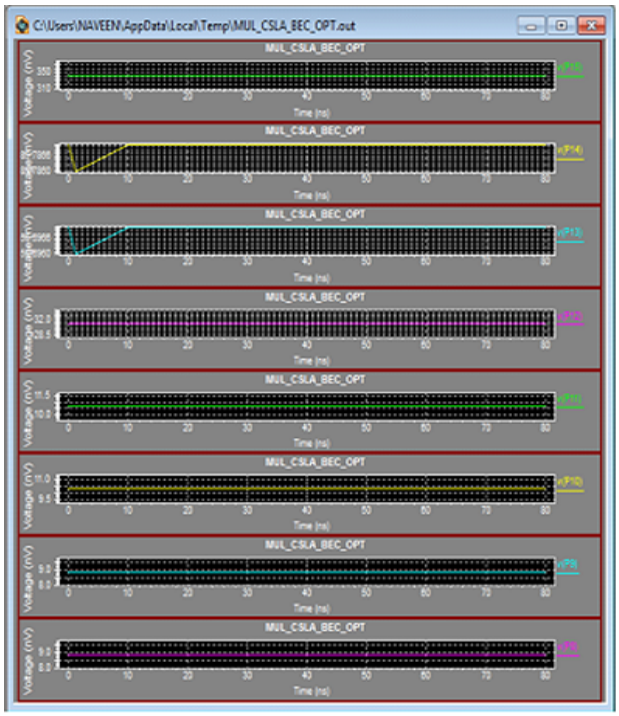


Table 7. Full Custom Results

DESIGN	POWER(watts)	No.of gates
MUL_RCA	2.138968e^-002	7692
MUL_CSKA	2.190428e^-002	7852
MUL_CSLA	3.231109e^-002	9396
MUL_CSLA BEC	3.020092e^-002	7896
MUL_SQRTCSLA	2.935139e^-002	8432
MUL_SQRTCSLA BEC	2.882727e^-002	8092

The multiplier using ripple carry adder consumes least power because of the less hardware utilised in the architecture. The multiplier using carry select adder consumes the most power. The proposed multiplier using square root carry select adder consumes less power than the multiplier using carry select adder.

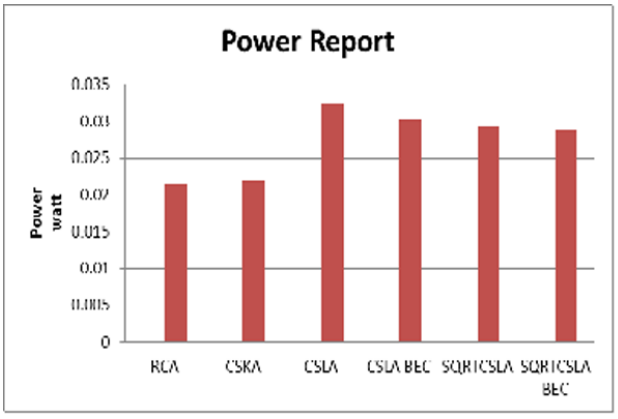


Fig. 48. Power Report

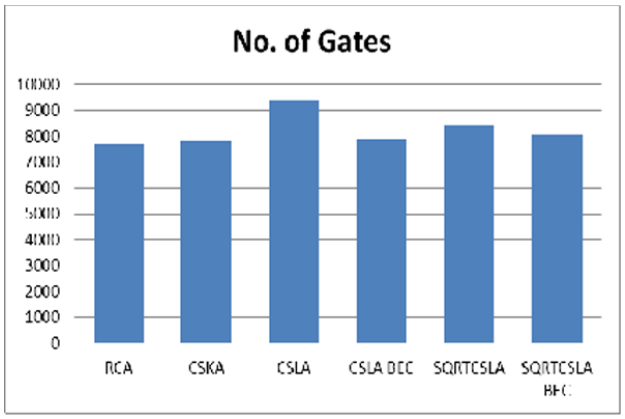


Fig. 49. No. of Gates

7. Conclusion

The vedic multiplier was designed using urdhavatiryakbhyam and implemented using semi-custom and full custom approaches. In the semi-custom approach the different proposed multipliers are realised in both Faraday's 180nm technology as well as in 65nm technology. The results of power, delay and area are analysed. From the result obtained from 180nm technology, the multiplier carry select adder reduces the delay when compared to the multiplier using ripple carry adder it consumes more power. But in fast-fast design corner the multiplier using modified carry select adder using BEC consumes almost 1mW power less than that of multiplier using carry select adder. The square root carry select adder is even better than these two designs consuming even less power and delay. The multiplier using square root carry select adder with BEC consumes only a slightly more power (600 µW) than the ripple carry adder with a slight increase in delay. But, when the designs are implemented in 65nm technology, the results are not very promising there is increase in both delay and power than the other designs. In the full custom design, the power alone is analysed. From the results, the multiplier using modified square root carry select adder with BEC consumes less power (3.4 mW) than the multiplier with carry select adder.

References

1. ShamimAkhter, "VHDL Implementation of fast NxN multiplier based on Vedic Mathematics," *IEEE*, ISBN: 978-1-4244-1341-6, ECCTD, 2007.

2. Kunchigi.V, "High Speed area efficient Vedic multiplier," *IEEE*, ISBN: 978-1-4577-1545-7,Mar. 2012.

3. HimanshuThapliyal and M. B. Srinivas, "High speed efficient NxN bit parallel hierarchical overlay multiplier based architecture based on ancient Indian vedic mathematics," *Transactions on Engineering computing and technology*, vol. 2, Dec. 2004, ISSN 1305-5313.
4. Y. He, C. H. Chang, and J. Gu, "An area efficient 64-bit square root carry select adder for low power applications," in Proc. *IEEE Int. Symp. Circuits Syst.,* 2005.
5. B. Ramkumar, H. M. Kittur, and P. M. Kannan, "ASIC Implementation of modified fast carry save adder," *Eur. J. Sci. Res.,*vol.2, 2010.
6. T. Y. Ceiang, and M. J. Hsiao, "Carry select adder using single ripple carry adder," *Electron. Lett.,* 1998.
7. O. J. Bedriji, "Carry select adder," *IRE Trans. Electron. Comput.,* pp. 340-344.