Journal of Engineering Science and Technology Review
Special Issue on Telecommunications, Informatics, Energy and Management 2019

JOURNAL OF
Engineering Science and Technology Review

Conference Article

www.jestr.org

ALL Digital PWM Control of a Three-Phase BLDC Motor

Anatoliy Aleksandrov, Goran Goranov and Pavel Hubenov

Department of Electronics, Faculty of Electronics, Technical University of Gabrovo 4 Hadji Dimitar street., 5300 Gabrovo, Bulgaria

Received 29 September 2019; Accepted 27 February 2020

Abstract

The brushless DC (BLDC) motor has found favor in applications as diverse as computer cooling fans, disk drives, cordless power tools, electric scooter or car, and record turntables. As prices continue to fall, the motors will find even wider use in all but the most price-sensitive applications. However, as demand increases, so too does the requirement for smoother, more efficient, and quieter BLDC motor operation.
While sinusoidal control is the best way to achieve these goals, it comes with extra cost and complexity relative to more traditional, trapezoidal control techniques. This paper will discuss BLDC motor control based on logic schematic implement in CPLD.

Keywords – PWM, control system, 3 phase inverters, CPLD, brushless DC motor, scooter.

1. Introduction

As implied by its name, brushless DC motors don't utilize brushes; motor movement is controlled by means of carefully designed drive signals. Compared to brushed motors, brushless motors offer improved reliability, longer life, smaller size, and lower weight. BLDC motors have become more popular in applications where efficiency is a critical concern and, generally speaking. A BLDC motor is considered to be a high-performance motor capable of providing large amounts of torque over a wide speed range [1].

Some BLDC motors use Hall-effect sensors for detecting the position of the motor's rotor with respect to the motor's stator. These advantages allow it to be used in electric scooters and cars. Generally, all modern adjustable control systems for 3 phase electric motors are based on the principle of pulse-width modulation, PWM [2]. Excluding case are soft starters which control is realized by smooth increase of the angle of duty cycle of the sinusoidal signals towards triacs.

Depending on the application of the motor, the requirements for the control system are extremely varied.

Starting from analogue electronic schematics (sinusoidal PWM, SPWM) and till digital PWM generators in embedded systems. [3, 4] Systems converting direct current to alternating current are labeled as inverters. These devices are used for precious control of electrical motors with different applications - water pumps or fuel combustion tank's pumps, cooling systems of automatic climate controls, built-in inverter in the pump itself with a remote control from a great distance, rapidly start-stop systems etc. All of them basically have been realized with PWM generator no matter of the approach - software language or electronic schematic. [5]

Some of basic parameters determining the concrete design are minimal and maximum frequency, minimum and maximum duty cycle, sampling rate, modulation index. Based on these parameters and their flexibility can be defined working ranges which to be compatible with a platform for implementation of the system.

The selected approach by the constructors depends on the system requirements. The variation shown in Fig. 1 is processing with analog input signals – control circuit generates a sinusoidal control signal, called the reference signal, and a triangular signal, called carrier. These control signals, which are synchronized, are compared by the comparator and providing PWM output signal. The disadvantage of the method is that any deviations or respectively interferences of both signals can cause missing of synchronization of the generators and will reflect on the output digital signal [6].

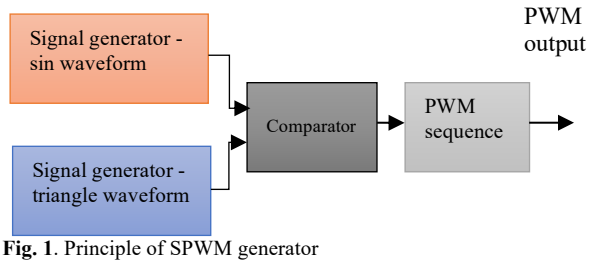

Fig. 1. Principle of SPWM generator

These disadvantages can be avoided by designing with digital generators which reproduce sawtooth form signal and another signal with square waveform with duty cycle 50 percent. Stability of the system can be significantly increased with next level approach of using software code and a specific platform. In case like that, used base frequency, which is the clock frequency of the platform, is in range of MHz, more stable compared with previous

* E-mail address: alex@tugab.bg
ISSN: 1791-2377

methods. Wide range of options available during designed - amount of blocks of code to check for deviations than the expected behavior as some internally checkpoints, feedbacks and so on.

The variants of decisions for the design of such a control system depend on the concrete application of the electrical motor.

For achieving of processing only with digital signals is presented a method with hardcoded times of the PWM output signal. The designed control schematic of the three-phase voltage source inverter is derived from SPWM principle. The inverter consists of three half-bridge inverters, which are connected in parallel and have the same phase output voltages with a phase difference of 120 degrees.

2. Design of PWM generator IN CPLD

Power switches of a three-phase H-bridge inverter is shown on Fig. 2.

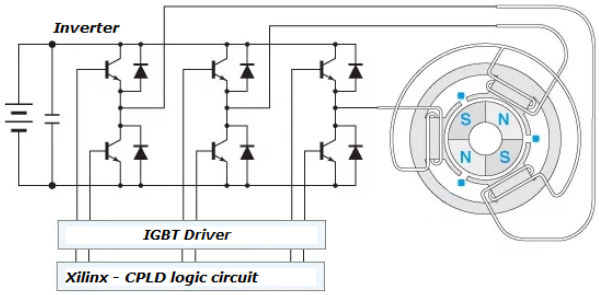

Fig. 2. Power switches schematic

The basic rule is that saturation of two switches in a single branch simultaneously is forbidden statement.

The three-phase H-bridge pulse-width modulation inverter waveforms for 120 degrees switch conduction is shown on Fig. 3. Within every π/3 period there are only two working power switches. The gating signals are performed as square waveform with duration 2π/3. The inverter output voltages are in the form of a square-wave and according to their Fourier series analysis they have low order harmonic components (i.e., harmonics near the fundamental component). A very costly and large low-pass filter has to be applied between the output of the inverter and the load. One appropriate solution to reduce the filter size and cost is using the SPWM control technique [7].

This means that to attenuate these unwanted harmonic components, the square waveform shown on Fig.3. has to be replaced with PWM signals. Since, there are always two PWM gating signals with π/3 offset, is necessary the system to control two PWM signal generators which signals have the same offset of 60° degrees.

A. Logic gates functions implementation

As we know, the pulse-width modulation signal is in function of base, carrier and reference signals. First period, labeled "0" out of *n*, is a pause from moment zero till first cross point of comparison. It is performed by a number of pulses of the base signal [8, 9]. These pulses can be converted in a time period by a counter which is limited from an adjacent feedback adjusted to the same number of the pulses. The second period, labelled "1" out of *n*, is a pulse with high amplitude which duration is till next cross point aligning falling edge of the pulse. This duration is achieved by a counter with feedback different than the previous one. The analyze of the rest pulses and pauses is similar to the end of the period. The common feature for all of them is the counter with several different feedbacks, Fig. 4. So, one standard counter is equipped with all possible feedbacks, which are optionally design with an input for activation, to cover the range with all possibilities.

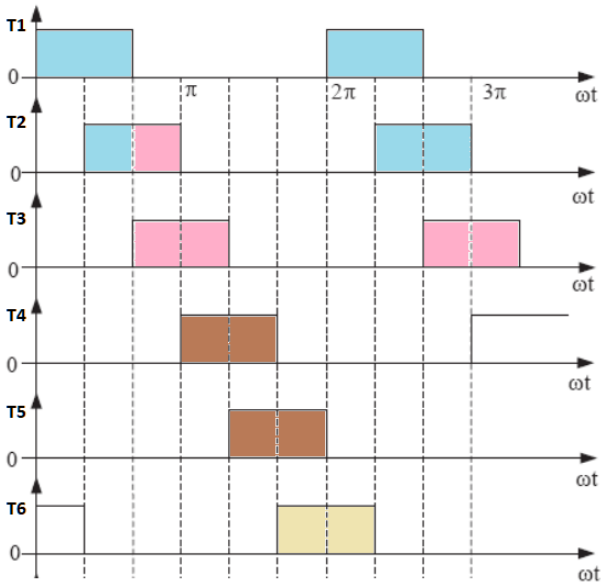

Fig. 3. Gating signals for switches T1 – T6

All feedbacks are collected with OR gate to reset the counter. This flexibility with one counter and all possible functions can be enlarged with few cascaded schematics. Then the total number the schematic can divide will be the multiplication of coefficients of every single counter. After the counter is designed is necessary to be triggered inputs for feedbacks activations. This functionality is guaranteed by a decoder which single active output will allow the appropriate counter's feedback, Fig. 6. For synchronous working of the counter and the decoder has to be ensured number of feedbacks to be the same as the number of the decoder's outputs. Following this purpose, the decoder is realized with two standard decoders with 16 outputs, managed by two counters [10].

The assembled schematic of the generator of pulse-width modulation signal is presented on Fig. 7. The initialization of the generator is consisting of reset of all modules in the beginning, arranged by the module "PWM_INPUT" when signal "CE", called Control Enabled, is set to "0".

When it is set to "1", decoder activates its own output number 0, which set to enable the connected feedback of the counter, which is already start counting. When counter reaches the moment to reset, the reset signal is delivered to the module "T_trigger_synchro_CLR" which trigger its state. That is required because reset signals of the counter are within short time. Processing in this way provides the output sequence after the trigger type T. [11]

When the generator is designed for 3 phase motor is necessary to double it for implementation. The 3 phase bridge branches are working in collaborative with two PWM generators with offset of 60°. This signal is provided from output "CS_60", called Control Signal of 60 degrees. The signal "CS_120" is with the same purpose. Both signals can be used as check points from the system.

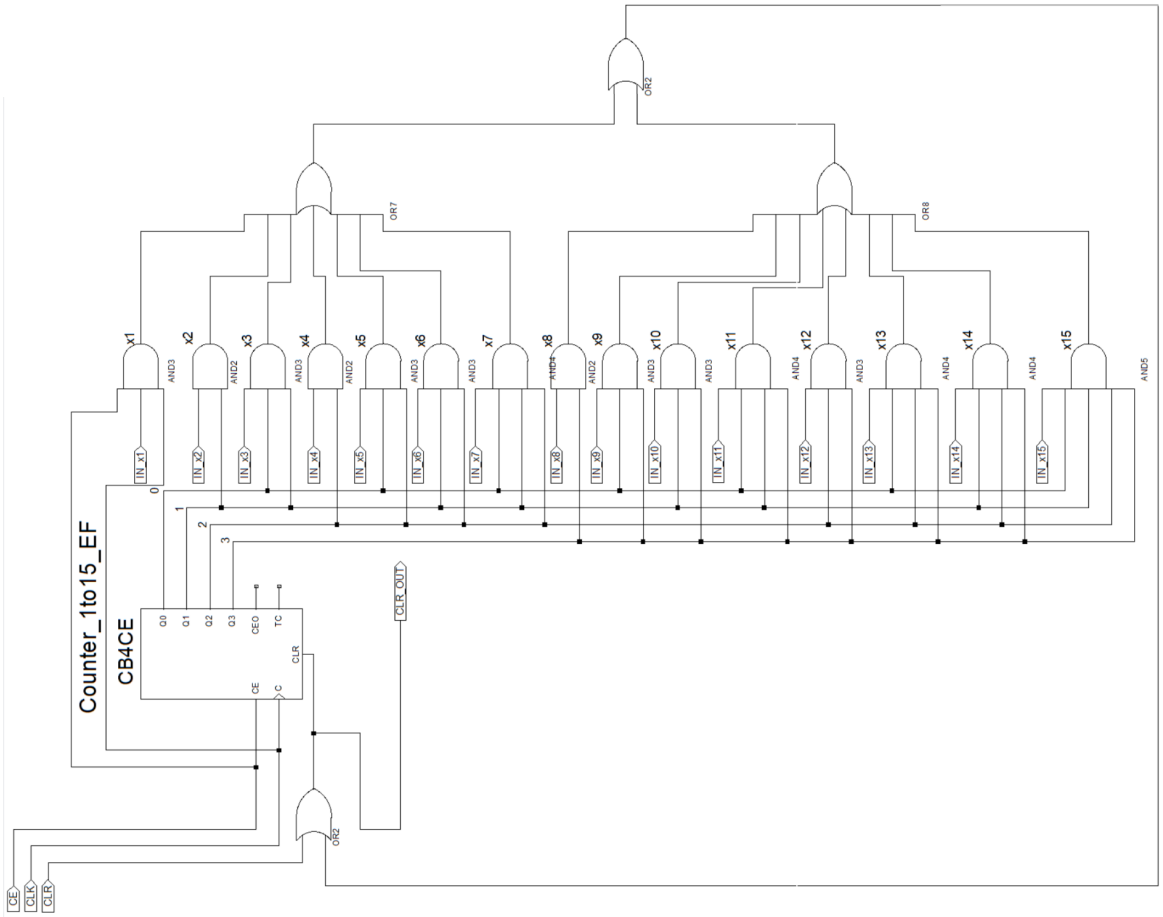

Fig. 4 Counter schematic with all possible feedbacks

B. *Calculations and block schematics*

For the following equations will be used an abstract diagram performing signals, their amplitudes and modulation index, Fig. 5 [12, 13]. The base signal with frequency fb used for all subsequent operations is presented with duty cycle 50%. This is the clock frequency of the CPLD circuit and is usually in range of MHz, applied 1MHz for this example. The ratio between the periods of the requested operating signal and the base one provides how many periods, respectively pulses N, are necessary to achieve it:

$$N = \frac{T_w}{T_b} \tag{1}$$

For T_w = 20mS (f_w = 50Hz) and T_b = 1μS (f_b = 1MHz) means that for a period of *fw* corresponds to 20,000 periods, respectively, of the base frequency [8].

Fig. 5 presents also the comparison about amplitudes between the carrier signal with frequency f_c and the desired working signal with frequency f_w. The correlation of their amplitudes is called a modulation index, *m*:

$$m = \frac{U_w}{U_c} \tag{2}$$

When *m* = 1, they are aligned as levels and systems enters in so called pre-modulation mode. This case has to be avoided. For this purpose, *m* = 0,8 is recommended.

The second dependence between the two signals is as follows:

$$f_c >> 10.f_w \tag{3}$$

The higher the f_c, the closer to the sinusoidal shape will be the sampling frequency. This significant difference also leads to a greater number of pulses in the PWM gating signal, which results in a larger occupied volume in the memory of used platform, but correspondingly less harmonics will be generated. Last but not least, there is the sound effect in coils of the electrical motor when operating, again higher frequency values are an advantage. The carrier frequency is usually selected to be 5KHz, 8KHz, 10KHz, 12KHz, or 15KHz.

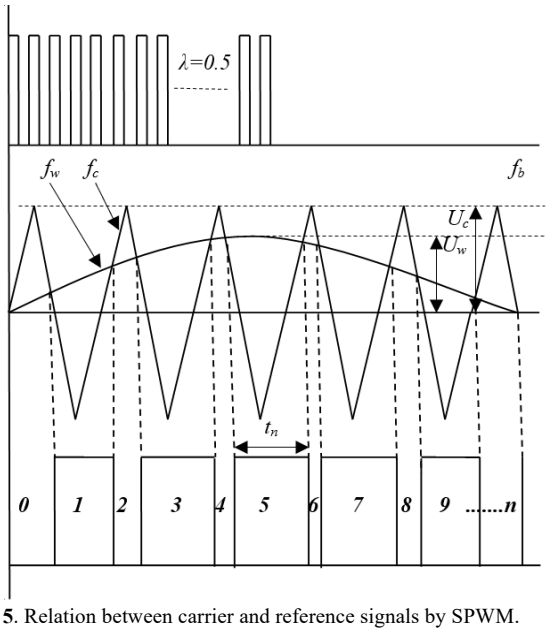

Fig. 5. Relation between carrier and reference signals by SPWM.

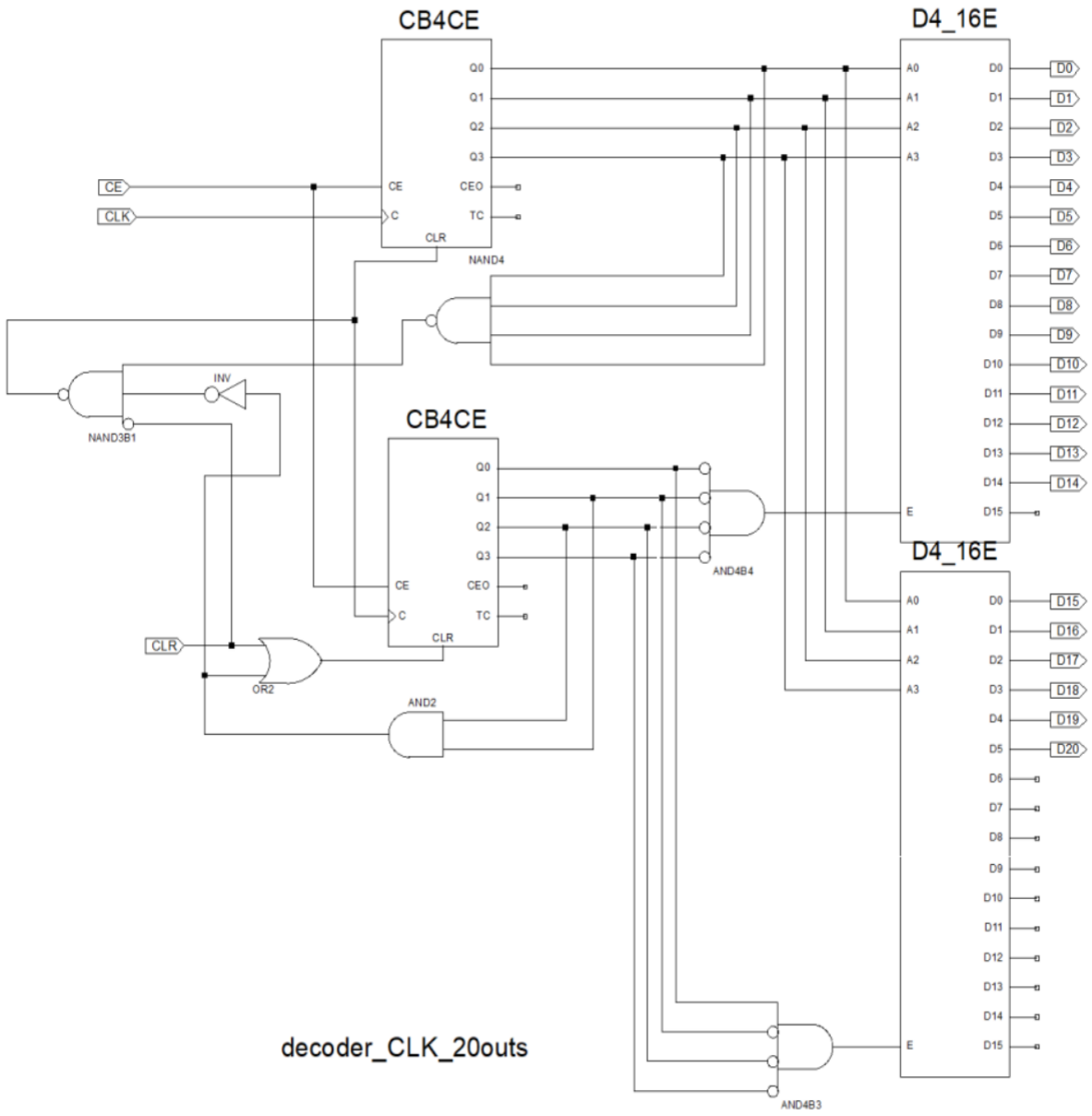

Fig. 6 Schematic of decoder with number of outputs in relation of number of counter's feedbacks

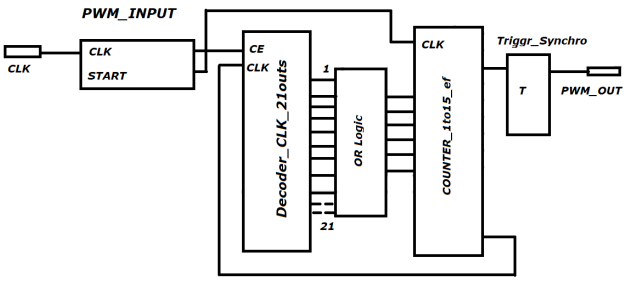

Fig. 7 Top level block diagram

The PWM signal axle is as a result of the determination of m, f_c, f_w, and the parameter t_n is obtained.
It shows how long the pulse or pause will be, depending on the sequence number n.

Since, there are too many numbers which has to be counted by a counter schematic, will be used an approach based on a counter with flexible feedback - Fig. 8. The base signal with frequency of the platform f_b is delivered to the input of the first counter. The counter is able to count to all necessary numbers, because all combinations from its own outputs are added to an OR gate. The decoder is used to activate in order the preliminary defined numbers of pulses as per the PWM output signal. Then every reset pulse of a counter triggers input pulse for the next counter. In this way, the pulse sequence with a strictly fixed duration is obtained for each consecutive pulse and pause, t_n.

The duration of the next pulse of Fig. 5 can be calculated by the formula:

$$t_n = a_1.b_1..x_n.T_b[s] \tag{4}$$

where a_1 is the value of the first feedback, b_1 the value of the second one, x_n is the value of the next in row feedback, T_b is the base signal frequency period. Thus, 6 cascaded in row counters with the same feedback set to 10, according to the formula will provide pause duration from Fig. 5:

$$t_0 = 10.10.10.10.10.10^{-6}[s] = 1\text{sec} \tag{5}$$

If on the next clock cycle, one of the counters is up to 5, is obtained for the duration of the following calculation:

$$t_1 = 5.10.10.10.10.10^{-6}[s] = 0.5\,\text{sec} \qquad (6)$$

Finally, the output PWM signal is formed by "T" trigger realized with "D" latch. It ensures proper duration of any coming short reset signal from last counter.

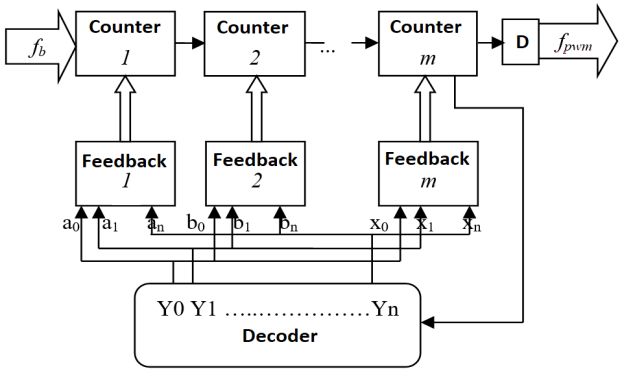

Fig. 8 PWM generator with flexible feedback

3. Conclusions

Advantage of the methodology is the simplicity of generating a PWM output signal with counter and decoder. Based on SPWM technique for accurate timings of pulse and pause. Using an internal generator for base clock signal with higher frequency increases the stability of the system. The presented equations are the basic dependencies when platform for realization is electronic schematic with logic gates functions. Accuracy of the output signal is in function of base and carrier signals which allows different decisions during design phase.

The illustrated approach of designing a generator with pulse-width modulation entirely using digital produced signals allows avoiding of any outside disturbances accompanying analog signal methods, and usage of any additional generators.

Main disadvantage of the mentioned PWM generator is lack of flexibility. Using hardcoded timings allows only changes about the input frequency of the base signal. Improvement of the flexibility requires more complex feedback and additional blocks, e.g. improving of the sample rate leads to add extra decoders with different numbers of outputs.

The approach of the control system of 3 phase electrical motor with fixed hardcoded timings allows the system to be designed and implemented sufficiently simply, efficiently and reliably. The platform compatible to the requirements is CoolRunner-II, with XC2C256-7TQG144C. Used matrix delivers flexible enough base for fine adjustments during the design of the system and subsequently in its implementation as control unit in real facility.

The illustrated methodology of designing a generator with pulse-width modulation entirely using digital produced signals allows avoiding of any outside disturbances accompanying analog signal methods, and usage of any additional generators.

The design combines mathematical model and synthesis through minimization of logic gate functions, which allows further expansion of the control system with more functionalities even if another one programmable matrix to be added. The implementation presents this approach applicable in almost all the developments of programmable logic controllers' series of leading manufacturers. The advantage is much wider audience, unlike using any other language for programming.

References

1. Aaron M. Harrington, Christopher Kroninger, Characterization of Small DC Brushed and Brushless Motors, Army research laboratory, ARL-TR 6389, Mart 2013.
2. Grasblum, Pavel, "Sensorless BLDC Motor Control Using MC9S08AW60", Freescale Semiconductor, Roznov pod Radhostem, 2007;
3. Prof. Dr. -I ng. J. M. Pacas, Prof. Dr. -I ng. R. M. Kennel, "Servo Drives State of the Art and Modern Developments", IECON 2005, Raleigh, North Carolina, USA, 6-10 Nov, 2005;
4. Karailiev, V., V. Rankovska, New approach for designing high-performance controllers in electrical drives systems using Programmable Logic Devices. ICEST 2013 Conference Proceedings, vol. 2, Ohrid, Macedonia, ISBN:978-9989-786-89-1. pp. 717-720.
5. NEC, "3-phase brushless DC motor control 120-degreee trapezoidal drive with hall sensors for MC-LVKIT-714 motor control evaluation system";
6. Peterchev, Angel V., "Digital Pulse-Width Modulation Control in Power Electronic Circuits: Theory and Applications", p.58;
7. S. Manias, "Power Electronics and Motor Drive Systems", Elsevier, ISBN: 978-0-12-811798-9, pp.329-340, 2017;
8. Nouman, Klima, Knobloch, "Generating PWM Signals with Variable Duty From 0% to 100%, Based FPGA SPARTAN3AN", Brno University of Technology, 2013;
9. Tamboli, Jagtap, Sutar , "Pulse Width Modulation Implementation using FPGA and CPLD ICs", 2012;
10. Maini, A.K., „Digital Electronics - Principles, Devices and Applications", John Wiley & Sons Ltd, ISBN: 978-0-470-03214-5, Chichester, England, 2007;
11. Agarwal, A., Lang, J.H., "Foundations of Analog and Digital Electronic Circuits", Elsevier, ISBN: 1-55860-735-8, San Francisco, 2005;
12. Bhargavi Nisarga, Daniel Torres, "Sensored 3-Phase BLDC Motor Control Using MSP430", Texas Instruments, Dallas, Texas, 2011;
13. Yaskawa America Inc., "AC servo drives, Product Catalog", 2011-2014;